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**14. ABSTRACT**

In this project we (i) developed an innovative method for the electron (hole) mobility enhancement using controlled modification of the phonon dispersion in nanoscale structures; (ii) carried out theoretical and simulation work for establishing the nanowire structure parameters required for the phonon engineered electron mobility enhancement; (iii) minimized the thermal resistance of the phonon-engineered structures to achieve better heat removal; and (iv) carried out proof-of-concept measurements for nanowire field-effect transistors demonstrating the mobility enhancement. On the final stage of the project, we built and investigated experimentally characteristics of a silicon nanowire (Si-NW) Schotttky-barrier (SB) MOSFETs. The dual-gated Si-NW MOSFETs have been fabricated by e-beam lithography on the highly-doped p-type substrate with $SiO_2$ layer serving as global back gate. We achieved the high ON current, high ON-OFF ratio and steeper sub-threshold swing. The mobility extraction employed TCAD Sentaurus device simulator to achieve higher accuracy. The temperature dependence of the carrier transport in NW FETs has also been investigated. All goals of the project have been successfully achieved. The demonstrated phonon and electron engineered nanowire transistors have such potential benefits as higher speed (electron mobility); better heat removal and thermal management; lower power consumption; smaller size and lower noise. The project contributions to the AFOSR mission include the foundation of an innovative technology, which can help to address the increasing need for the integrated multi-modal sensing and reliable communications. Two PhD graduate students involved in the project defended their dissertation and accepted employment at Intel Corporation and Texas Instruments.

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# Technical Details

## Executive Summary

We investigated characteristics of the silicon nanowire (SiNW) Schotttky-barrier (SB) MOSFET device, and extracted the experimental values of the mobility with the help of TCAD simulations. The dual-gated SiNW MOSFETs were fabricated on the highly doped p-type substrate with $SiO_2$ layer serving as the global back gate. We have found significantly increased ON current, high ON-OFF ratio and steeper sub-threshold swing. For mobility extraction we employed TCAD Sentaurus device simulator to determine the capacitance, which gives more accurate values as compared to any analytical formula. We also investigated the temperature dependence of the carrier transport in NW.

## I. Background

Quasi one-dimensional (1-D) field-effect transistors (FET), such as Si nanowire FETs [1] (Si NW-FETs), have shown promise for more aggressive channel length scaling, better electrostatic gate control, higher integration densities and low-power applications. At the same time, an accurate bench-marking of their performance remains a challenging task due to difficulties in definition of the exact channel length, gate capacitance and transconductance. In 1-D Si FETs, one also often observes a significant degradation of their mobility and on/off ratio. Recently SB MOSFETs are widely studied for the possible application in nanoscale logic application as a alternative to traditional MOSFET where highly doped source and drain form ohmic contact to metal silicide [2]-[6] due to their immunity to short channel effect [7]-[10]. In this project, we investigated the hole mobility of SB Si NW.

## II. Device Fabrication Technology

We prepared SiNWs by Au-catalyzed vapor-transport as described in Ref. [11]. This method allows one to grow Si/SiO2 core/shell NWs with a ratio of roughly 1:1 between the crystalline

core radius and the oxide shell thickness. Unlike SiNWs grown by chemical-vapor deposition, where a ~1-2 nm thick native oxide layer is formed upon exposure to atmosphere [11], our thick oxide shell arises from phase-separation of SiO into Si and $SiO_2$ when the precursor vapor condenses to form SiNWs at temperatures around 800 °C [11],[12] . In this study, we used SiNWs with core 7-10 nm radius and shell of 7-10 nm. The overall NW diameter is thus in the 25-40 nm range, as can be deduced from the SEM image in Figure 1 micrograph showing the core/shell Si/SiO2 structure of our SiNWs. After synthesis, SiNWs are mechanically transferred onto a 300 nm thick $SiO_2$ layer thermally grown on top of a heavily p doped Si wafer, used as bottom gate. The substrate-which we refer to back gate - is used to control the electrostatic in the contact region. FET terminals of desired geometries are then defined on top of individual SiNWs by e-beam lithography. E-beam Evaporation of 70/50 nm of Ni/Au is carried out for source/drain electrode in $10^{-6}$ torr right after 10 s BOE dip for oxide removal in the contact regions. This step (placing the sample in ebeam evaporator quickly and pump it down just after oxide removal to prevent re-oxidation in ambient) is crucial for good electrical contact in source/drain region. In the last step, an aligned second step non-overlapping Ti/Au (70/50 nm) top gate is defined. Devices are characterized at this stage and also after annealing.

## III. Silicide Formation

Our devices are annealed at 400 °C in $N_2$ for 4 min prior to measurements. References 13 and 14 pointed out that upon annealing Ni can diffuse in the SiNW to form silicide contacts. Ref 13 reported that this effect is significant for annealing temperatures as low as 290 °C, we have also found similar effect that around 500 nm of exposed section of our NW is converted to nickel silicide at 400 °C shown in Figure 2.

## IV. Electrical Characteristics

The electrical measurements were performed with a probe station coupled with Agilent B1400 A device analyzer which has 1 fA current resolution. Figure 3 shows transfer characteristics of devices measured before and after annealing. Devices with unannealed contacts always behave

as p-channel enhancement mode (normally off) FETs; at $V_g$ =0 V, current is only tens of femto amperes (instrument limited). The p-type behavior is attributed to accumulation of holes in a SiNW channel, while the normally off behavior at $V_g$ =0 is attributed to carrier depletion caused by the Schottky barriers. At 400 °C a dramatic transition to ambipolar behavior is observed. Such behavior requires both source and drain contacts with low barrier heights for majority and minority carriers, which can be switched between n channel and p channel. Therefore, the transition from unipolar p channel to ambipolar is attributed to significant improvement in contacts by annealing. Moreover, the p-type behavior can be explained by the different transmission of electrons and holes through the SBs. This is given by the smaller SB heights for holes than for electrons in combination with the band bending at the SBs. The SB height between n-type bulk Si and Ni-silicide is typically 0.66- 0.75 eV for electrons and 0.39-0.48 eV for holes in p-type Si, these values are reported to be relatively insensitive to the Ni-silicide phase involved [15],[16] but can change when the Schottky contact is scaled down [17]. Moreover the resulting band bending at the Schottky contacts caused by the applied electric gate field could adjust the carrier transmission through the SBs and determine which type of carriers can pass more easily. Owing to smaller SB height for hole from silicide to valence band of silicon, it is more favorable for holes to contribute to current. One of the most significant differences between fully-gated NWFETs or NTFETs and conventional MOSFETs is the frequently observed ambipolar behavior in the $I_{ds}$-$V_{gs}$ characteristics as shown in the Figure 3. We can create this undesired characteristic in our devices by using the back gate alone. However, our design also allows us to obtain excellent unipolar device characteristics as shown in Figure 3. By applying a constant back gate voltage of $V_{BG}$ = −40V and sweeping the top gate, hole injection from the source is enabled while electron injection from the drain is suppressed at the same time.

It is more desirable during operation to switch the FET using the top-gate, as the better coupling ensures lower threshold voltages and steeper subthreshold slopes. Figure 4 plot transfer curves ($I_{ds}$ vs gate voltage) recorded by sweeping $V_{TG}$, while $V_{BG}$ is kept at -40 V (left) and +40 V (right), respectively. In all cases, $V_{DS}$ is set to 50 mV. For this SiNW, the corresponding inverse subthreshold slopes [$dV_{TG}/d(\text{Log } I_{DS})$] for hole and electron accumulation are 90 and 450 mV/decade, respectively with the $I_{on}/I_{off}$ ratio of $10^7$ and $10^5$ for p-type and n-type regime respectively.

To estimate the field effect mobility, TCAD simulation was done by Synopsis [18] Sentauras. This can estimate the capacitance more accurately than any analytical formula. Here the Poisson equation was solved together with drift diffusion equation to solve the electrostatic profile. For the correct simulation, the diameter and the gate thickness was determined from the SEM of cross section of the nanowire done by Focus Ion Beam. Figure 4 (left) shows the cross section of the NW the circle is 15 nm that the diameter of the NW in this case with 5 nm of $SiO_2$ wrapping around it and Figure 4 (inset) is the electrostatic potential profile for this structure. Figure 5 gives the estimate of the simulated C-V profile for the top gated SiNW. Figure 6 shows that the analytical formula $C=\frac{2\pi\varepsilon_r\,\varepsilon_o L}{cosh^{-1}\,(1+\frac{2t_{ox}}{d_{ox}})}$ gives incorrect estimation for the same geometry (5 nm $SiO_2$ wraps around the NW of various diameter) because in reality the top gate covers around 80 percent of the circumference on the NW.

Now we assess the field effect mobility for hole. We restrict our mobility extraction to holes since holes have small SB height than that of electrons and gives reasonable transconductance value. The transconductance can be written as $g_m=\frac{dIds}{d\,Vgs}|_{Vds}$ where $V_{ds}$ is low bias (In this case $V_{ds}$=50 mV). The analytical expression for mobility is $\mu_p = g_m \ \frac{L^2}{C_{ox}}\frac{1}{V_{ds}}$. The length was taken as the top gate length since the underlapped regions are converted to nickel silicide. Figure 7 shows $\mu_p$ as a function of top gate $V_{gs}$. The peak mobility was found around 260 $cm^2/Vs$. It can be observed that the field effective mobility at first increases with the vertical electric field due to a decrease in the Coulomb scattering, but then decreases for large vertical fields due to the enhanced surface scattering and contact resistance associated with the Schottky barriers to the higher subbands.

## V. Effect of Temperature on Silicon Nanowire Transport

We have investigated the effect of temperature on the carrier transport in Si NW devices. As the temperature is increased we expect that conductivity will decrease due to increased phonon scattering. But since we have SB FET the injection of carrier first increases as the thermionic emission goes up for hole as we increase the temperature from ambient to 50 °C. Even the carrier scattering is increases in the NW but the total number of carrier increases and thus

conductivity increase. But after the phonon scattering dominates and current reduces. In the figure 8 the effect of temperature on conductivity shown. The figure 8 shows the hole transport varying the temperature. The back gate is kept at -60 V to inject holes from the contact. As hole has lower SB height conduction is almost Ohmic. But there is non-linearity due to the thermionic emission. For hole the current show an increment from RT to 50°C as thermionic emission increases the hole injection even though the mobility is reduced by phonon scattering. After that we see decrease in current due to phonon scattering. Figure 9 shows the $I_{ds}$-$V_{ds}$ for electron transport at various temperature. Since SBH is higher for electron the current monotonically increases as temperature is increased owing to more and more thermionic emission of electron. Table 1 summarizes some of the important parameter in the state-of-the-art Si-NW devices.

**Table 1**

| | This work | Walter et al | Byon | Cui | Appenzeller | Colli | Lu |
|---|---|---|---|---|---|---|---|
| Ref. | | 14 | 21 | 20 | 13 | 19 | 22 |
| active region | i-Si | i-Si | i-Si | i-Si | i-Si | i-Si | i-Si |
| Lg (μm) | 0.7 | 0.67 | - | 0.8-2 | 0.5 | 3 | 1 |
| Diameter (nm) | 20 | 20 | 20 | 70 | 60-90 | 20-30 | 20 |
| Ron [Ω] | 66 K | 625 K | 15 M | 1.1 G | - | 10 M | 2.7 M |
| Ion/Ioff | $10^7$ | $10^7$ | - | - | - | $10^6$ | |
| SS swing (mV/dec) | 85 | - | - | - | 140 | 135 | - |

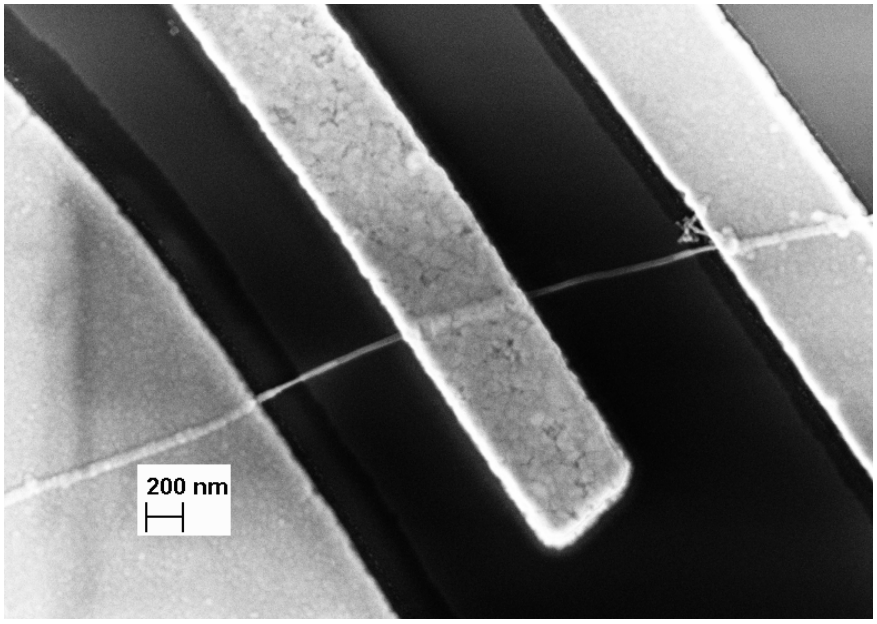


Figure 1: SEM image of a Si NW FET. The scale bar is 200 nm.

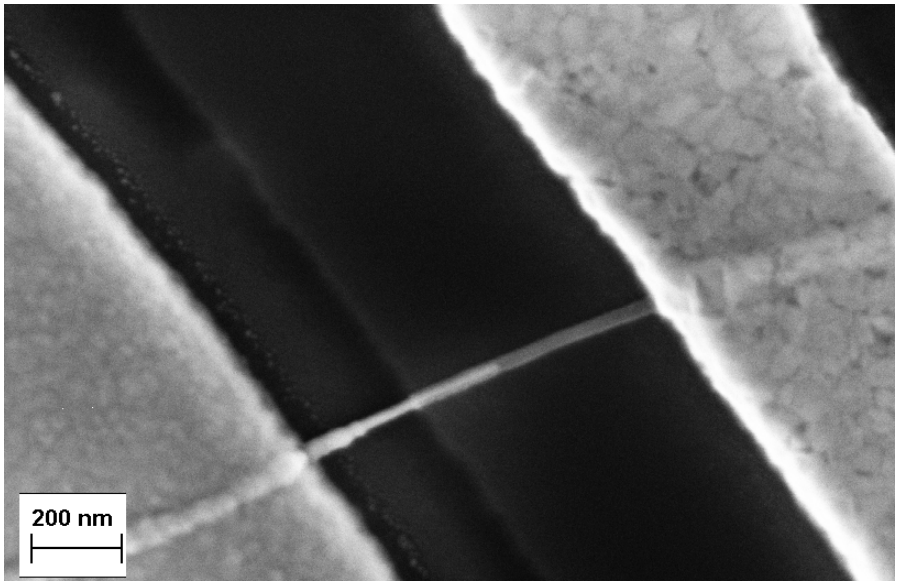


Figure 2: SEM image of a Si NW after annealing at 400 °C for 4 minutes. The scale bar is 200 nm.

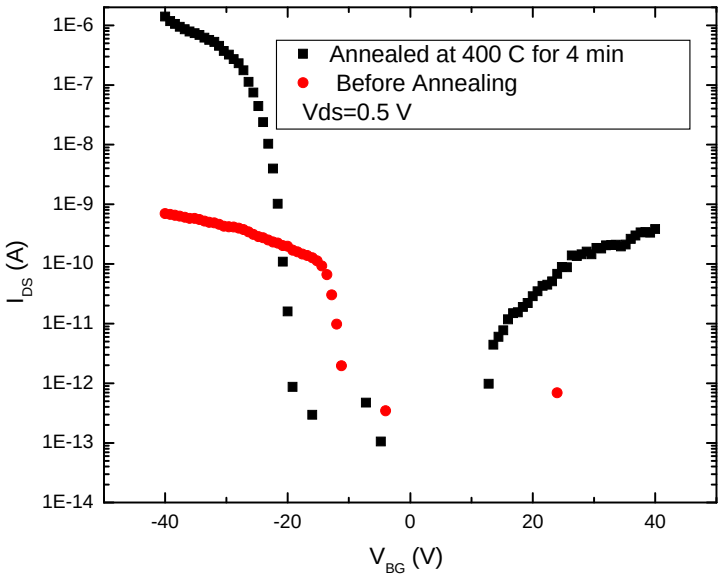


Figure 3: Transfer characteristics of a back gated SiNW FET. The red curve is before annealing showing p-type unipolar behavior, and the black curve is after annealing at 400˚ C for 4 minutes showing the ambipolar behavior.

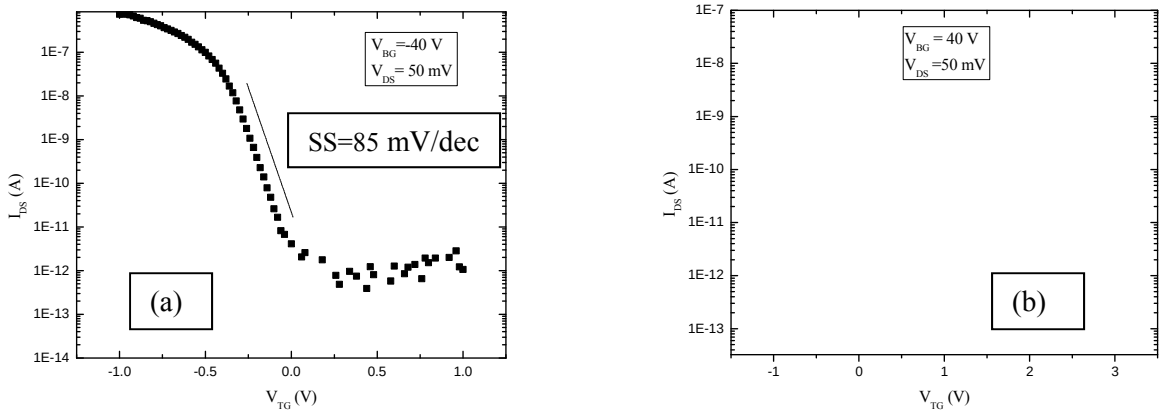


Figure 4: Unipolar sub-shreshold characteristics of a SiNW FET. P-type regime (left) N-type regime (right).

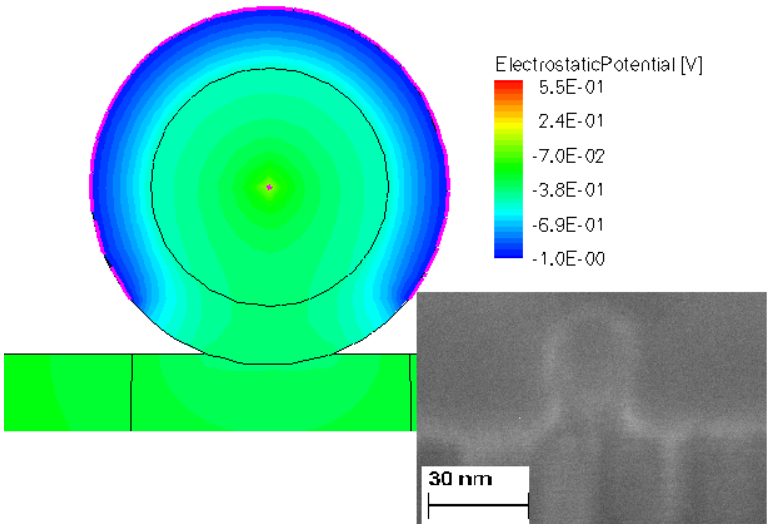


Figure 4 (C): SEM iamge of X-section of SiNW under the top gate (inset).Electrostatic profile of simulated NW under the top gate.

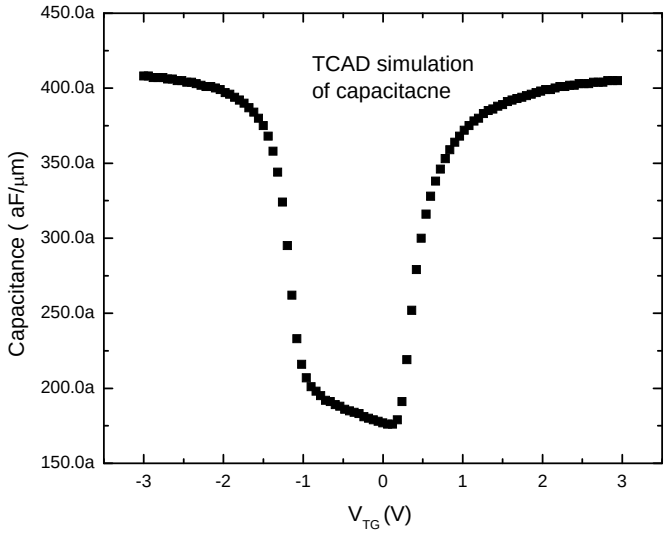


Figure 5: Simulated C-V characteristics of top gated SiNW.Top gate is varied from -3 to +3 V while back gate is kept at -40 V.

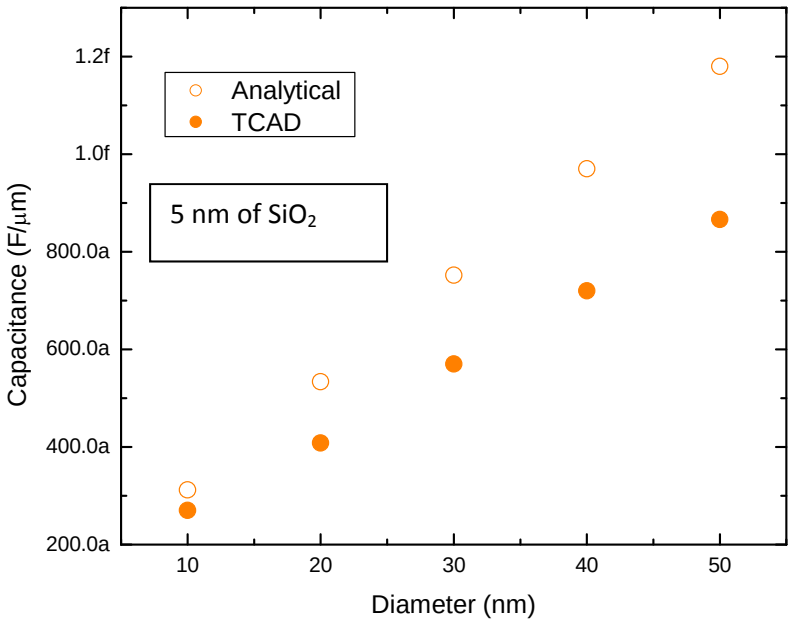


Figure 6: Comparison between extracted capacitance using analytical formula and TCAD simulation.

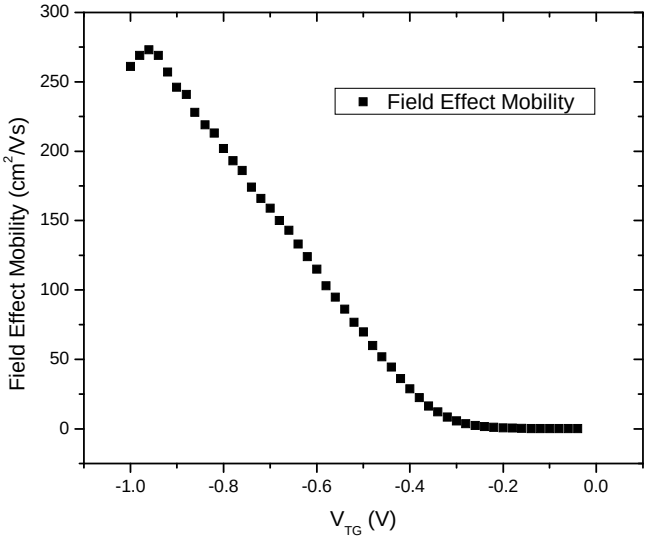


Figure 7: Field effect mobility (hole ) as a function of top gate Vgs. Note that the Ids-Vgs plot was smoothed before the transconductance , $g_m$ was calculated for field effect mobility assessment.

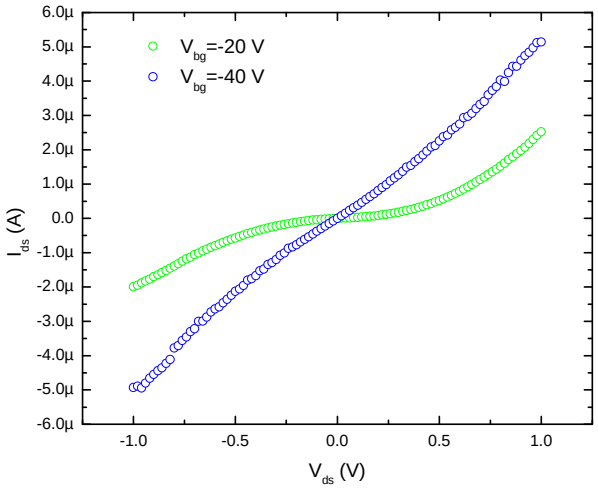


Figure 8: $I_{ds}$-$V_{ds}$ curves at different back gate voltage showing Schottky contact turns to Ohmic contact for holes for sufficient back gate voltage.

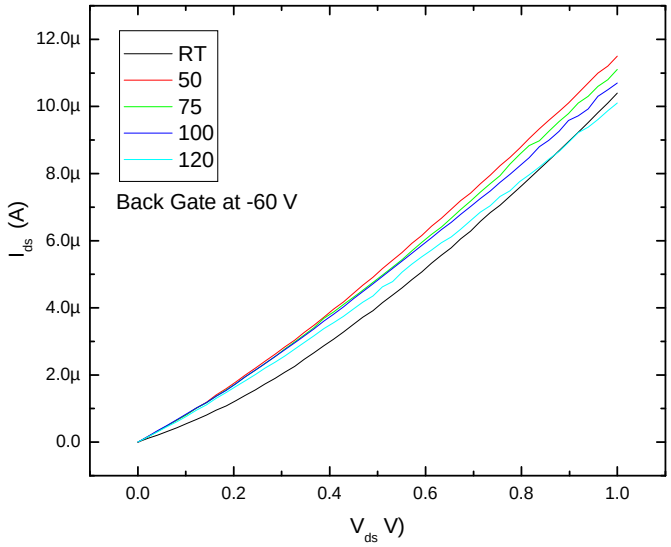


Figure 9: Ids-Vds curve at back gate -60 V. Temperature varied from RT to 120 °C.

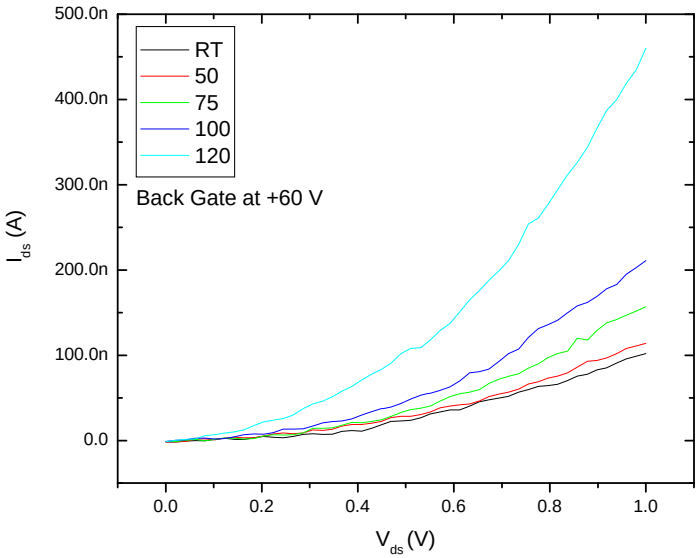


Figure 10: Ids-Vds curve at back gate +60 V. Temperature varied from RT to 120 °C.

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# Phonon Engineered Si Nanowire Field-Effect Transistors with Enhanced Performance

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Quasi one-dimensional (1-D) field-effect transistors (FET), such as Si nanowire FETs (Si NW-FETs), have shown promise for more aggressive channel length scaling, better electrostatic gate control, higher integration densities and low-power applications. At the same time, an accurate bench-marking of their performance remains a challenging task due to difficulties in definition of the exact channel length, gate capacitance and transconductance. In 1-D Si FETs, one also often observes a significant degradation of their mobility and on/off ratio. The goal of this study is to implement the idea of the FET performance enhancement via phonon engineering [1], while simultaneously performing a more rigorous data extraction. To achieve these goals, we fabricated dual-gate undoped Si NW-FETs with various NW diameters and gate dielectric materials (e.g. $SiO_2$, $HfO_2$ and $Al_2O_3$). The SiNWs are grown by Au-catalyzed vapor-transport [2]. For devices with $HfO_2$ and $Al_2O_3$ gate dielectrics, the original $SiO_2$ shell been removed with HF and then Al2O3 or HfO2 were deposited with ALD. When a proper combination of NW channel–gate coating radii, and channel–gate dielectric acoustic mismatch are found, one can expect an improvement in the transistor performance due to reduction in the electron–phonon scattering rates [1]. For our top-gate NW-FET, the subthreshold swing was determined to be 90 mV/dec, whereas the best subthreshold swings for Si NW-FETs until now were ~135-140 mV/dec [3,4]. We achieved a ON/OFF current ratio of $10^7$ due to improved electrostatic control and electron transport conditions inside the channel. This is on the higher end of any ON/OFF ratios thus far reported for NW FETs [4]. The hole mobility in our NW-FETs was around 300–400 $cm^2$/Vs, according to different extraction procedures. In our mobility calculations we included the NW silicidation effect, which reduces the effective channel length. We calculated the top gate capacitance using TCAD Sentaurus simulator, which gives more accurate value of capacitance of the NW over any analytical formulas. The same measurement routines were repeated for NW channels coated with $Al_2O_3$ and $HfO_2$. We will present a detail comparative study of the intrinsic properties of Si NW with different gate materials. We will show how drift mobility and other intrinsic properties are affected by the interface quality and acoustic mismatch (i.e. the product of the mass density and the sound velocity in the given materials). A strategy for further improvement of the NW-FET performance via phonon engineering will also be outlined.

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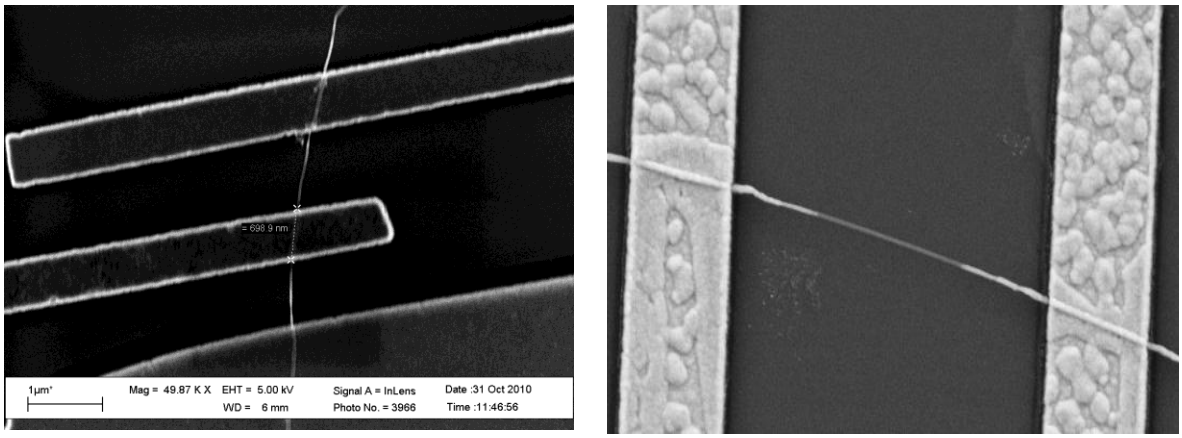



Figure 1: (left) SEM image of the top gated Si NW-FET; (right) silicidation of Si NW due to annealing at 400˚ C for 4 minutes.

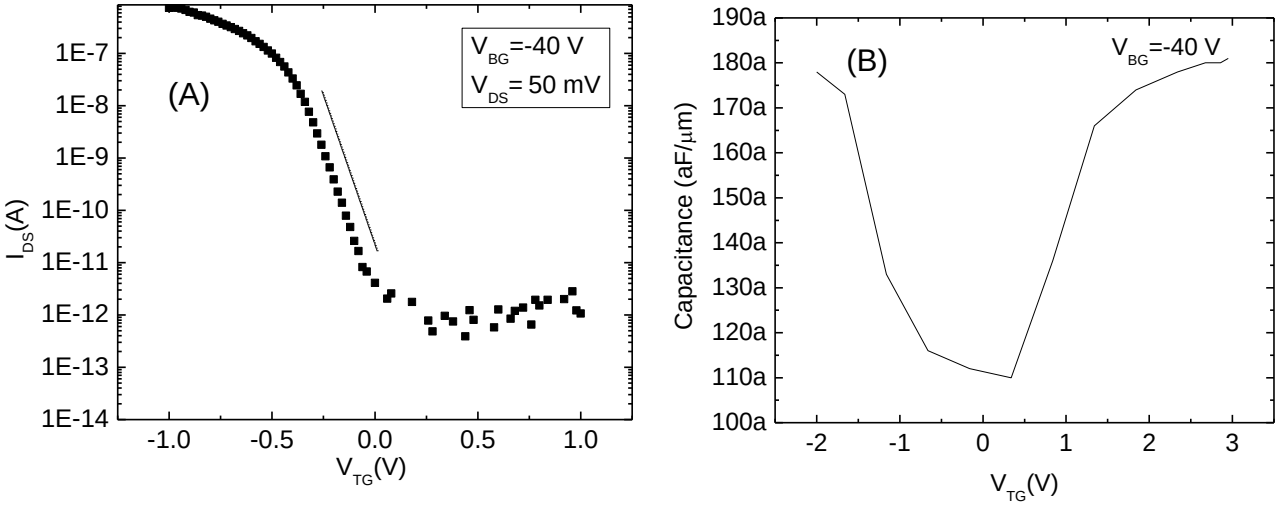



Figure 2: (a) Drain current vs top gate voltage and (b) simulated capacitance vs top-gate voltage. For this simulation, the cross-section of the nanowire underneath the gate was taken into account as the top-gate metal does not surround the whole nanowire.

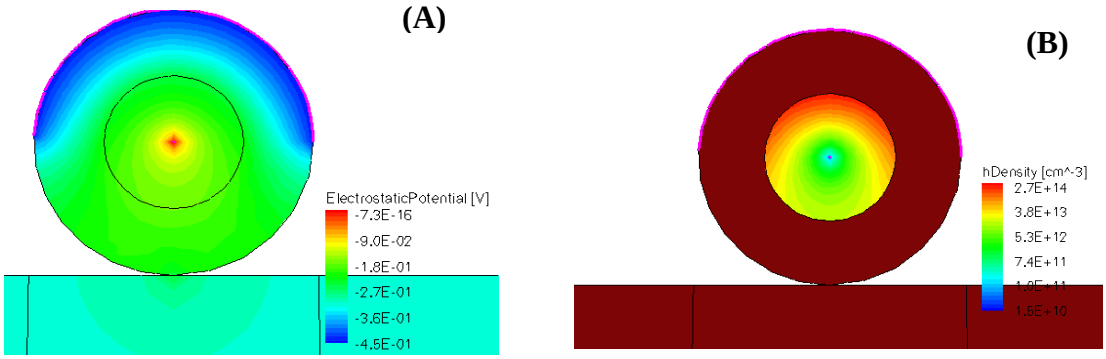
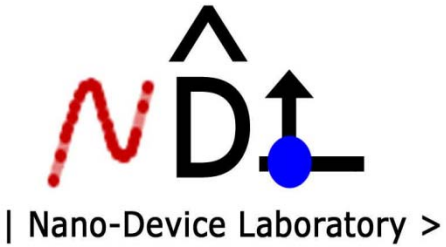



Figure 3 : TCAD simulation showing (a) electrostatic potential profile and (b) hole distribution around the NW.





# Fabrication and Characterization of High Performance Silicon Nanowire Field Effect Transistors

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**Nano-Device laboratory**
**Department of Electrical Engineering**
**University of California, Riverside**

# Outline

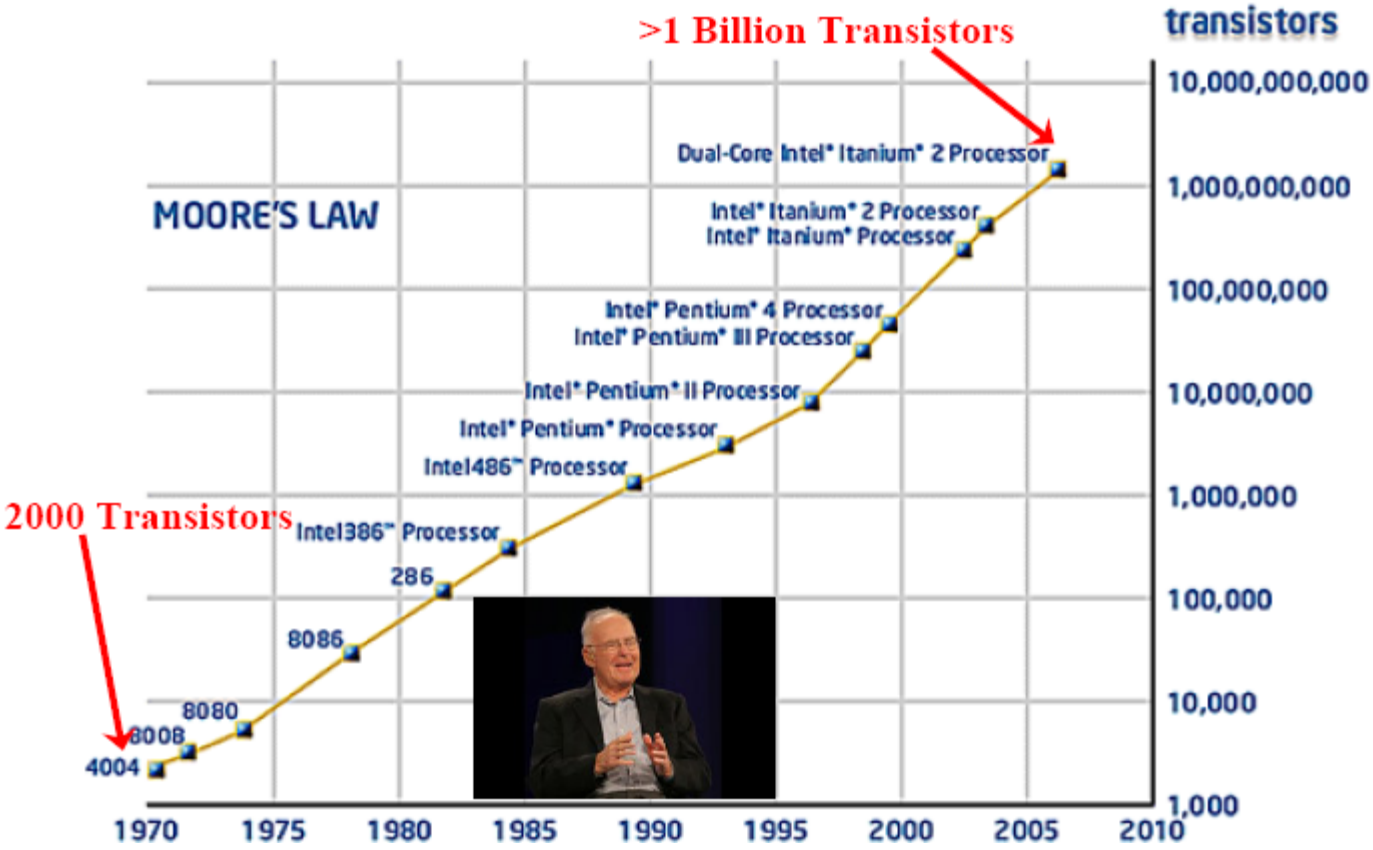
*Motivation*
- Technology Trends
- Why Nanowire

*Silicon Nanowires FET*
- Growth of NW
- FET Fabrication
- Electrical Characterization
- Simulation for Data Extraction

*Tunneling FET*
- Motivation for TFET
- Current TFET status
- Schottky Contact TFET

*Summary*

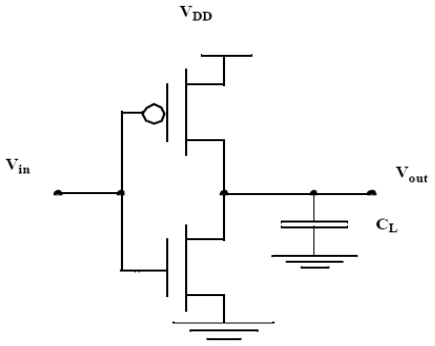
# Introduction: Historical Perspective




Number of transistor count doubles every 18 months
Ref: Gordon Moore ISSCC 2003

# Motivation/Limitation for Scaling

CMOS Inverter




$$I_{DS} = \mu C_g \frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$$

**Faster intrinsic speed of the MOS transistor leads to faster circuit.**

**Smaller transistor size saves real estate in chip that contribute to more transistors to increase functionality**

1. With increased clock frequency Dynamic power goes up.

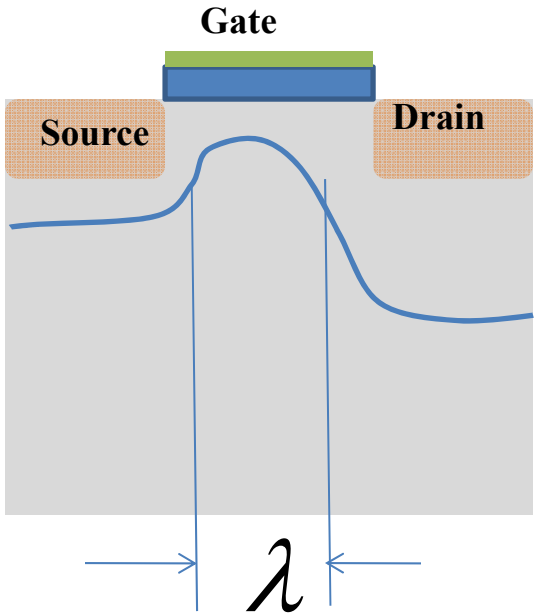
$$P_{Dynamic} = CV_{DD}^2 f$$

2. Leakage Power goes up.
   a. Gate insulator leakage
   b. Threshold leakage
   c. Source to Drain tunneling
   d. Drain to body tunneling

**Severe Short Channel Effect hinders scaling**

# Planar vs NW comparison

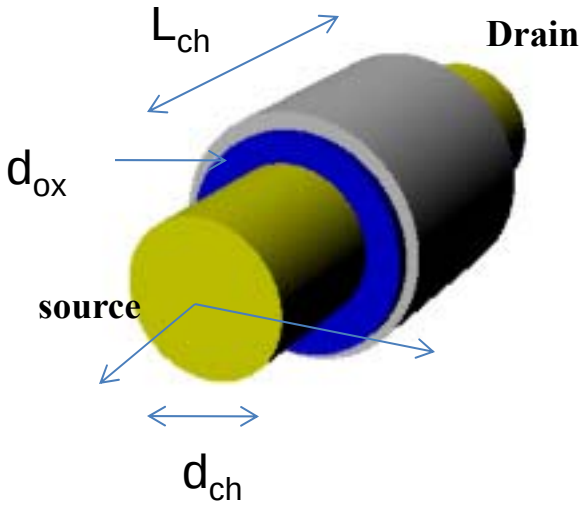
Planar MOSFET




Planar Geometry: Limited electrostatic control of the channel

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon ox} d_{ox} d_{ch}}$$

Nanowire MOSFET




NW Geometry: ultimate electrostatic control of the channel

$$\lambda = \sqrt{\frac{\varepsilon_{nw} d_{nw}^2 \ln(1+\frac{2d_{ox}}{d_{nw}})}{8\varepsilon_{ox}}}$$

**To avoid schort channel effect Lg>4λ**

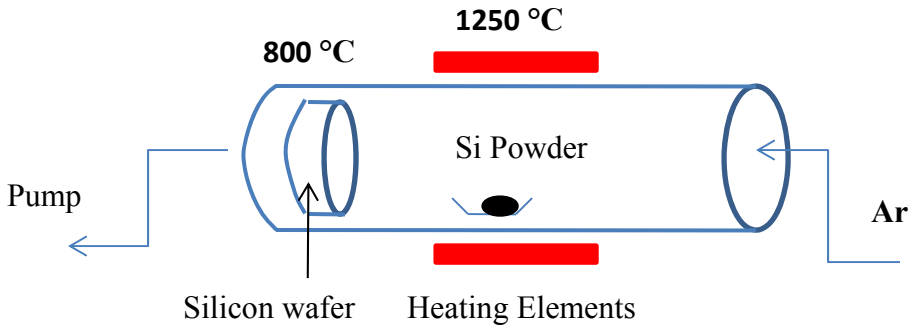
Example: 8 nm SOI 1 nmSiO2 gate λ=5 nm Lg>20 nm

Example: 8 nm dia NW 1 nmSiO2 gate λ=2.3 nm Lg>9 nm

# Silicon Nanowire Growth

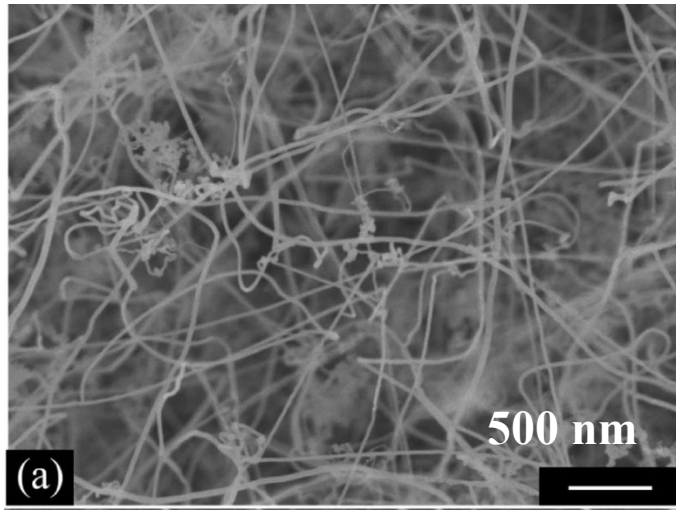
## Vapor Transport Growth

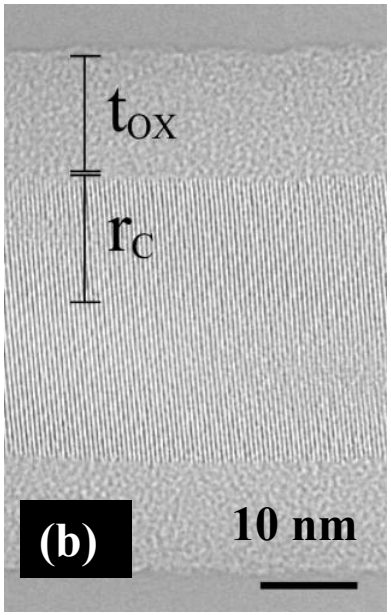
- Silicon Substrates are with 0.5 nm of Au ( 99.99 % ) in Ebeam evaporator at a base pressure below $10^{-6}$ mTorr. Thickness of the metal monitored by in situ quartz crystal.
- SiNWs grown on Au-coated Si substrates by vapor transport, with the Si powder temperature ~1250 °C
- Si substrate is kept at 800 °C in Ar gas
- The NWs are tens of microns in length, and their average diameter is between 20 and 30 nm.
- Thick oxide shell arises from phase separation of SiO into SiO2 and Si when the precursor vapor condenses to form SiNW at temperature around 800 °C

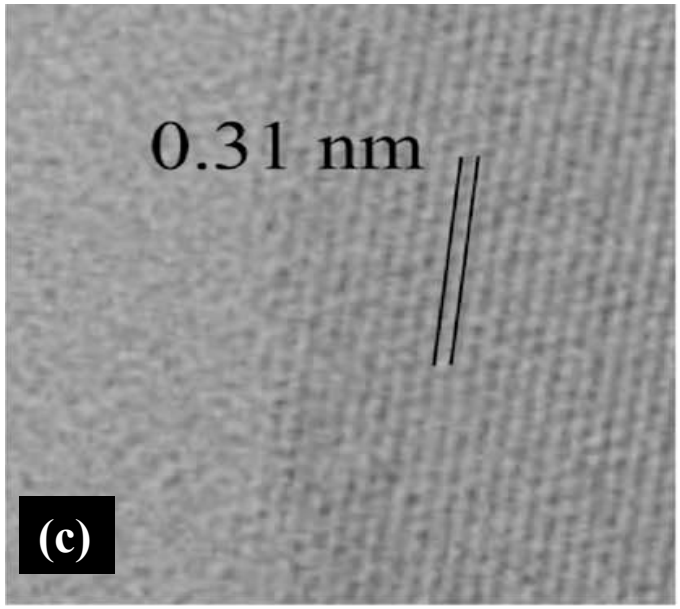



**Schematic of Furnace Tube**

# Characterization of Silicon Nanowire



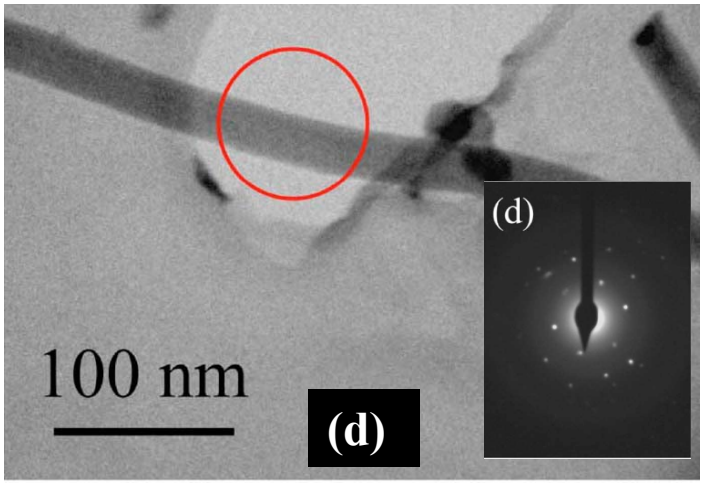
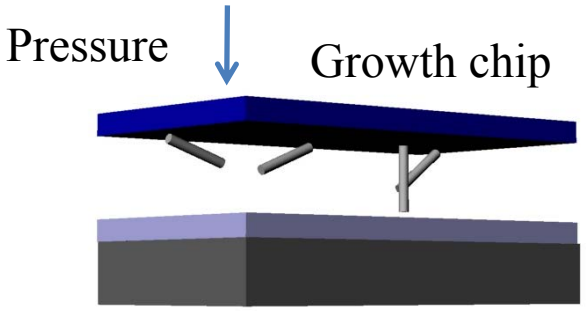




**Figure: (a) SiNWs grown on Au-coated Si substrates at 800 °C by vapor transport (b) High-resolution TEM micrograph of a SiNW showing the crystalline core and the thick amorphous shell (c) high resolution TEM image showing lattice (d)TEM of a single NW inset the selected area diffraction pattern (red circle is showing the selected area)**

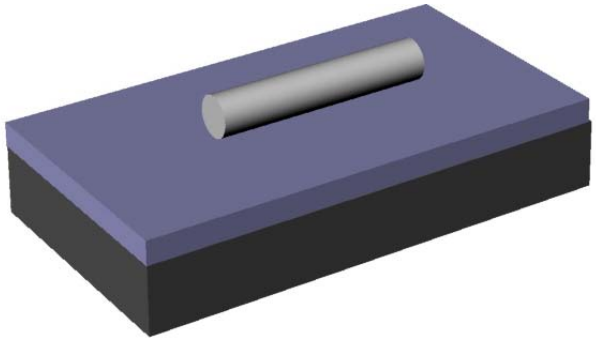
Ref: Colli, A.; Fasoli, A.; Beecher, P.; Servati, P.; Pisana, S.; Fu, Y.; Flewitt, A. J.; Milne, W. I.; Robertson, J.; Ducati, C.; De Franceschi, S.; Hofmann, S.; Ferrari, A. C. Thermal and Chemical Vapor Deposition of Si Nanowires: Shape- Control, Dispersion and Electrical Properties. *J. Appl. Phys.* **2007, *102, 034302.***

# Fabrication of Silicon Nanowire FETs

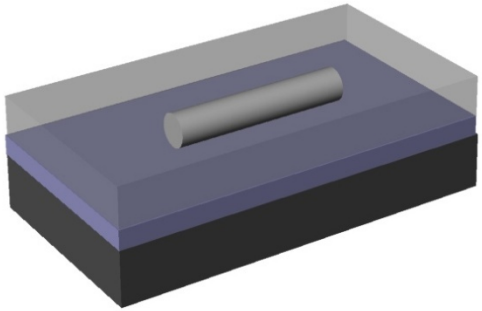



**(a) Mechanical transfer from the growth chip to device chip**

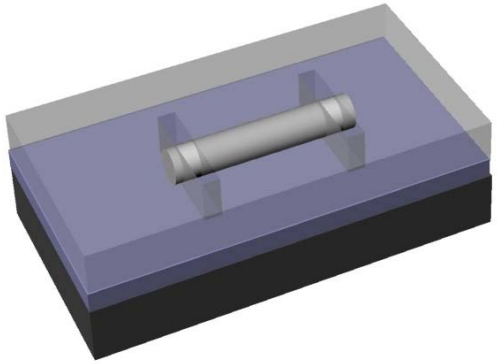
**300 nm thermally grown $SiO_2$ on degenerately doped p type substrate which is Au coated in backside serves as back gate**



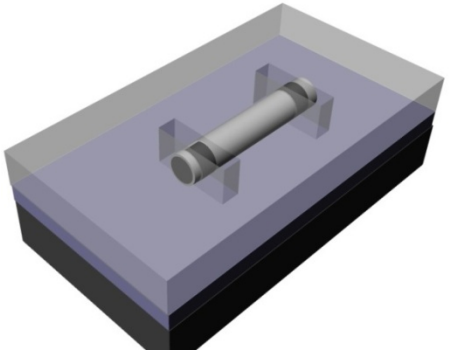
**(b) Nanowire is indentified through SEM or dark field optical microscopy**



**(c) layers of MMA (methyl methacryllate) and PMMA (poly methyl methacryllate ) are spun on the substrate.**

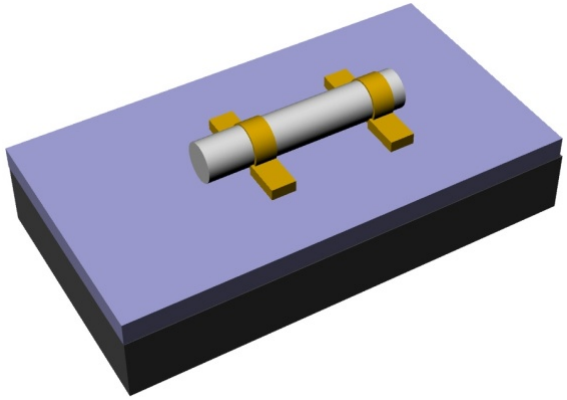


**(d) First Electron Beam Lithography to open Source and Drain contact**

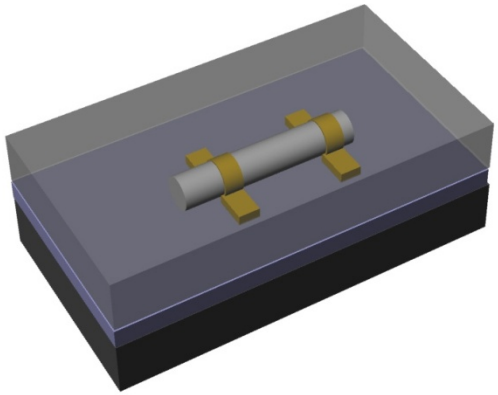


**(e) 10 s of Buffer Oxide Etch is done to remove shell oxide (critical step to obtain good electrical contact)**

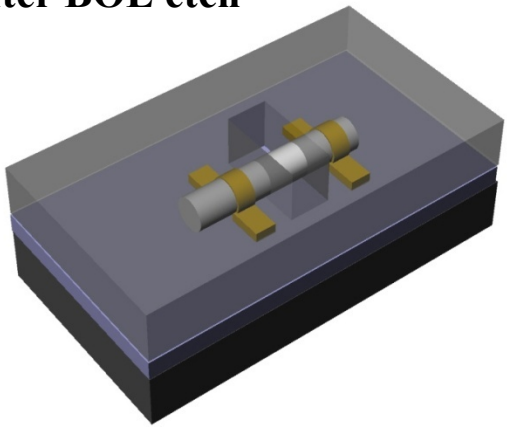
# Fabrication of Silicon Nanowire FETs



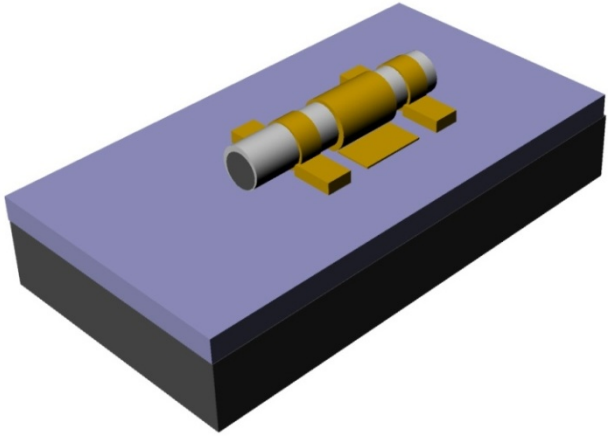
**(f) 70 nm of Ni is evaporated followed by 50 nm of Au in Electron beam evaporated in $10^{-6}$ Torr base pressure right after BOE etch**



**(g) Another layer of MMA and PMMA are spun on the substrate for second EBL for gate opening**

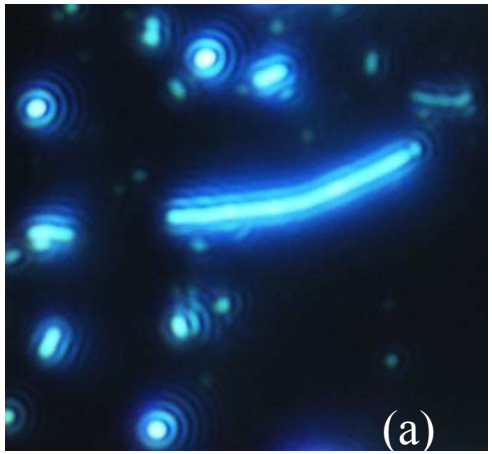


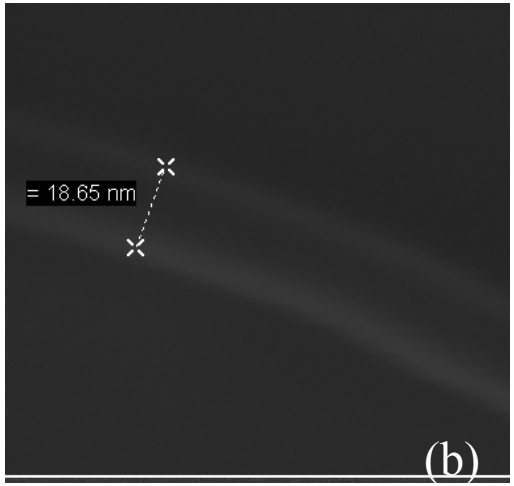
**(h) Second aligned EBL is done for top gate**



**(g) 70 nm of Ti evaporated followed by 50 nm of Au in Ebeam evaporator for final Dual gate SiNW FET**

# Fabrication of Silicon Nanowire FETs



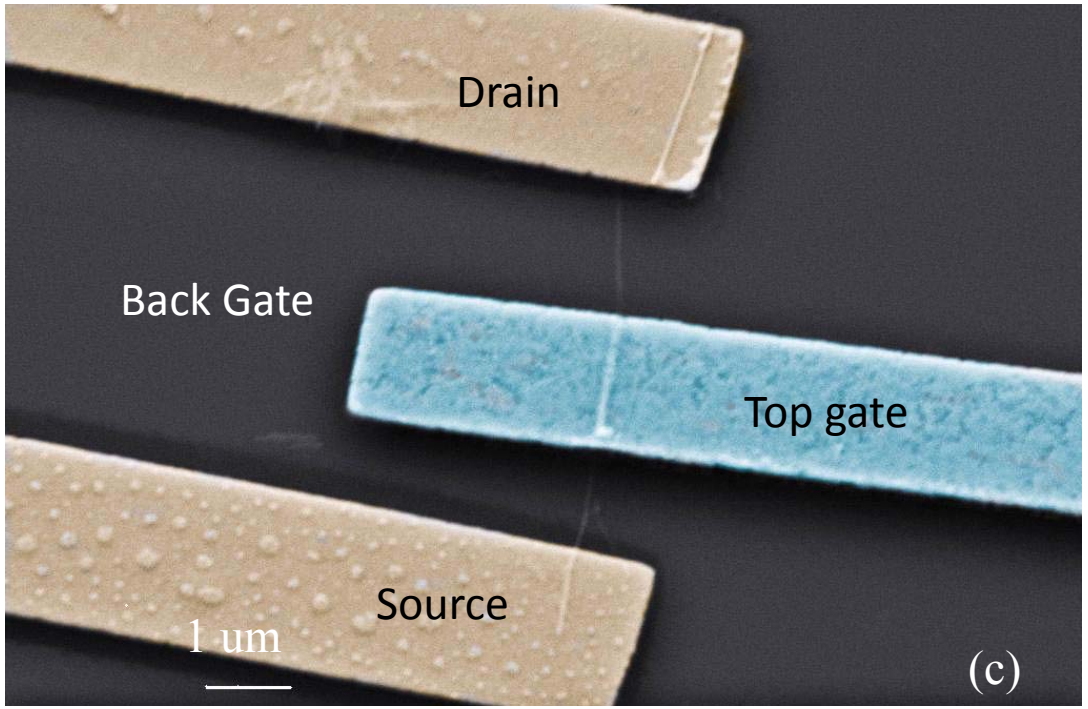
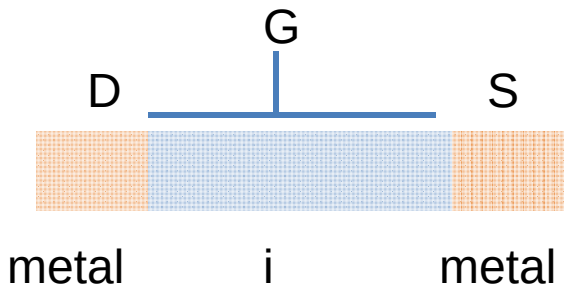
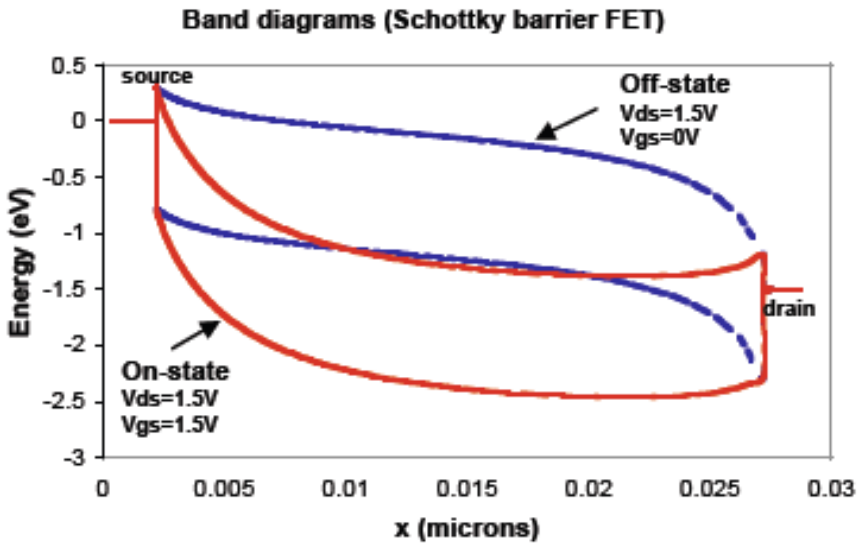




**Figure: (a) Dark Field image of Silicon nanowire (b) Scanning Electron Micrograph of Silicon nanowire (c) SEM image of dual gated Silicon nanowire (false color used to show source, drain and top gate)**

# Schottky- Barrier FETs



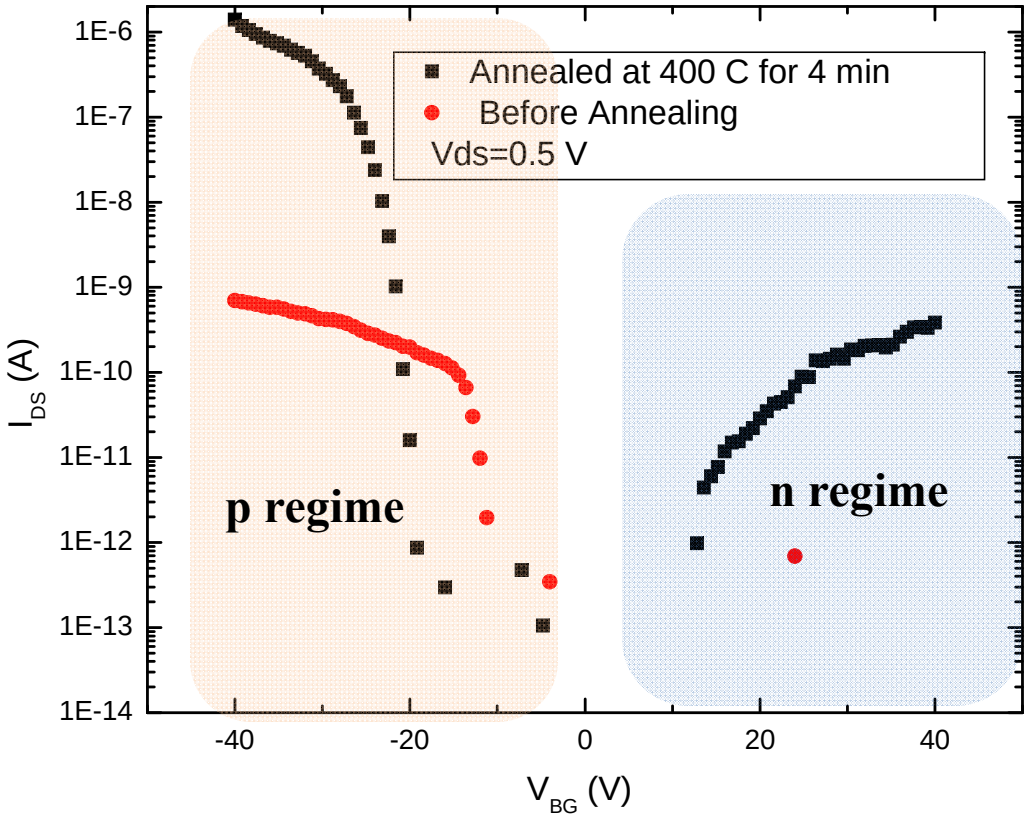

**Possible advantage of SB FET**

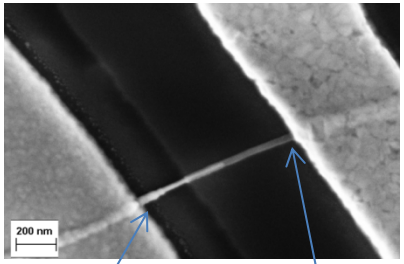
1. High doping of S/D not required
2. At High Vg >Barrier thin >Tunneling current high >Ion high
3. At Low Vg >Barrier thick > Tunneling current low >Ioff low

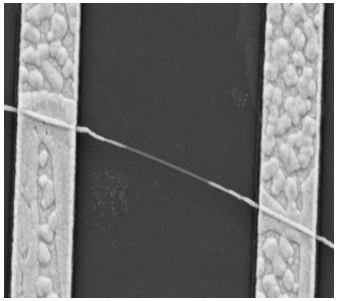
**Possible disadvantage of SB FET**

**Ion reduction due to Schottky barrier**

# Silicidation: Effect of Annealing



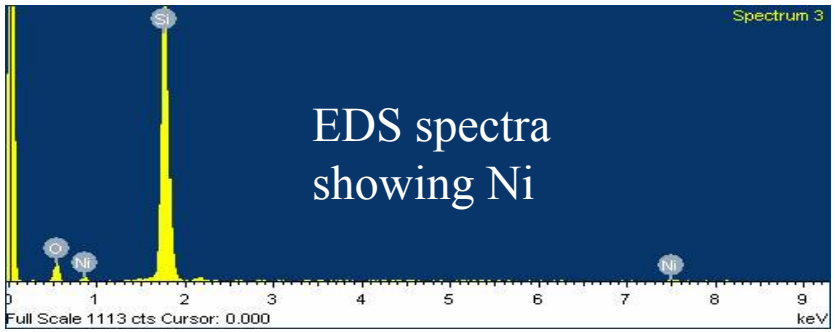



**NiSi due to annealing**

**No silicide as no annealing done**

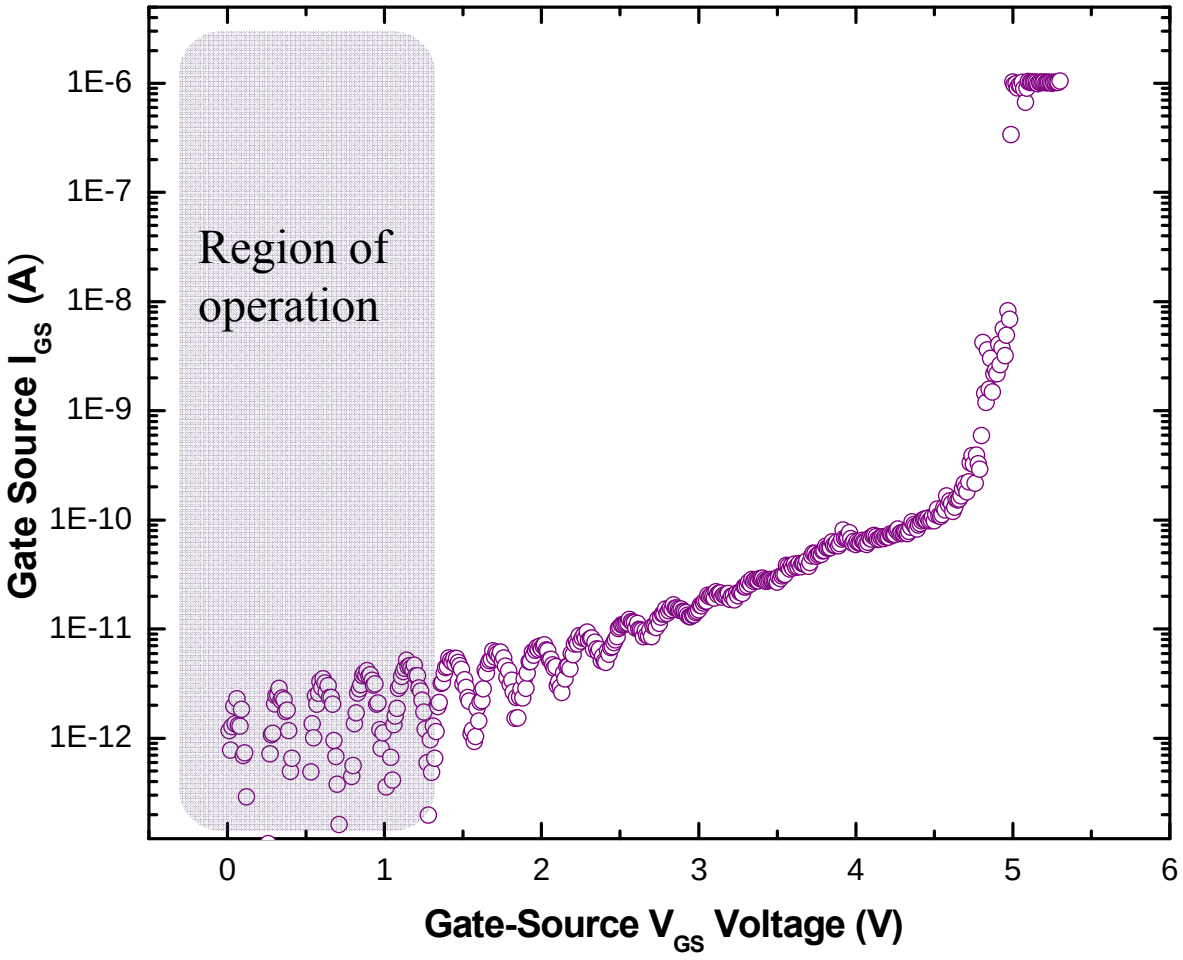
**NiSi silicide forms at 400˚C and penetrated into the nanowire unlike to planar device.The penetration depends on annealing temperature,time and diameter of NW.In this case 400˚C annealing for 4 min leaves 500 nm of exposed NW to be silicided**

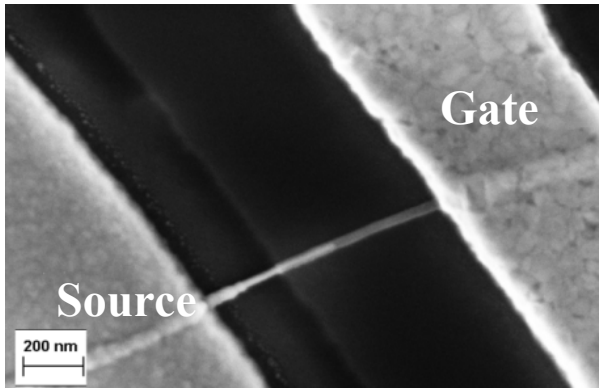



EDS spectra showing Ni

Ref: Appenzeller, J.; Knoch, J.; Tutuc, E.; Reuter, M.; Guha, S.Dual-Gate Silicon Nanowire Transistors with Nickel Silicide Contacts. International Electron Devices Meeting 2006, 1-2,302–305

# Gate Oxide Quality

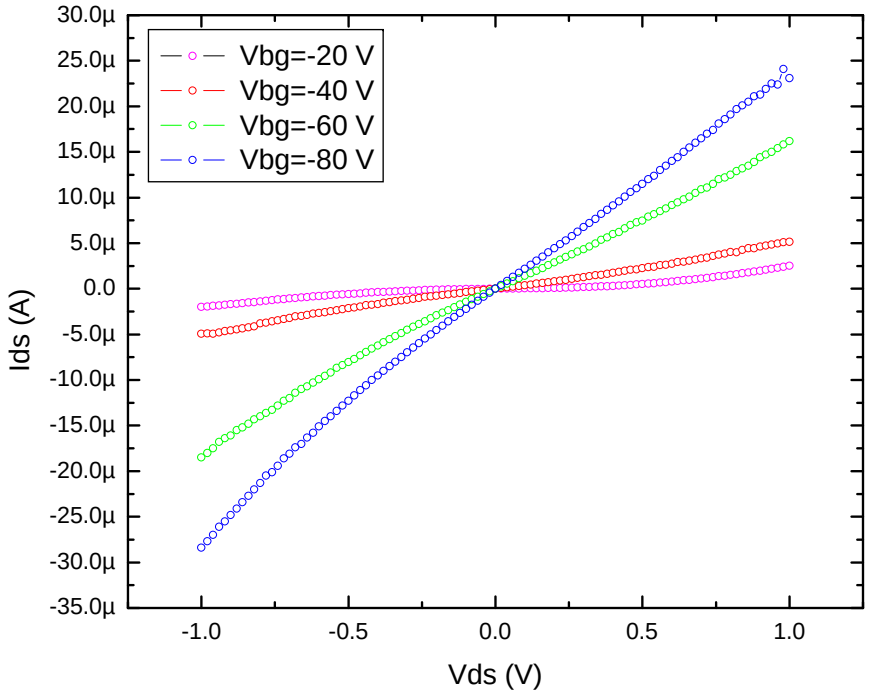


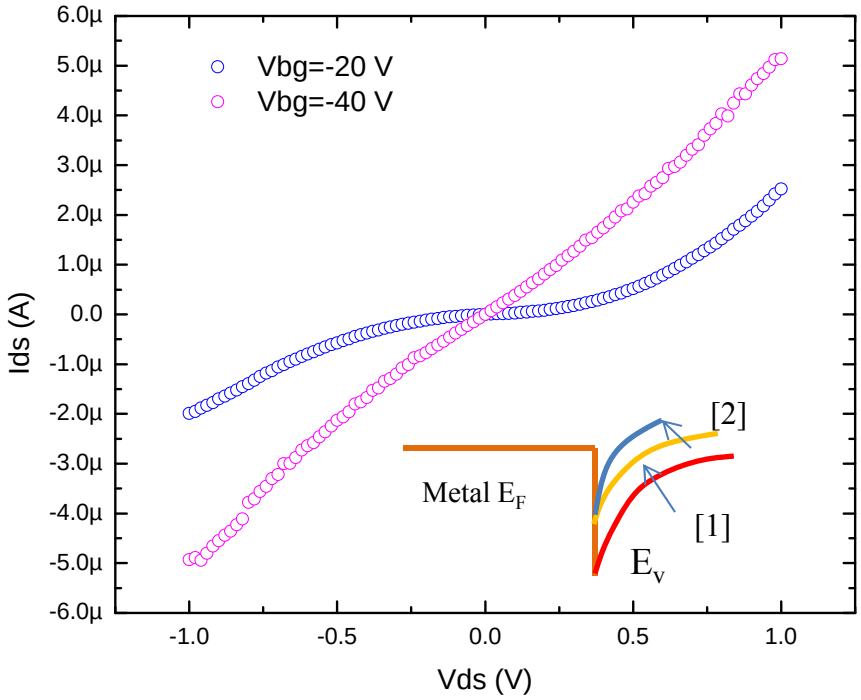




**Gate Oxide Break down voltage is around 5 V for 5 nm of SiO2 gate which corresponds to a breakdown field of $10^7$ V/cm. This matches with standard CMOS gate oxide breakdown [1] indicating high quality of the gate oxide**

[1] S M Sze. *Physics of Semiconductor Devices*, 2nd ed

# $I_{ds}$-$V_{ds}$ Characteristics of SiNW



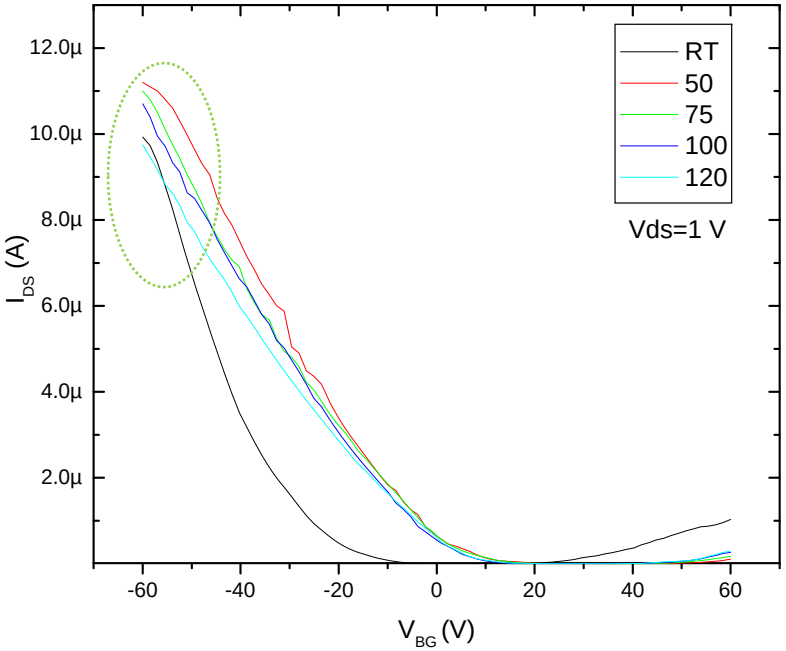

**Barrier Lowering due to electric potential by back gate** $\Delta\Phi = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}}$ [1]

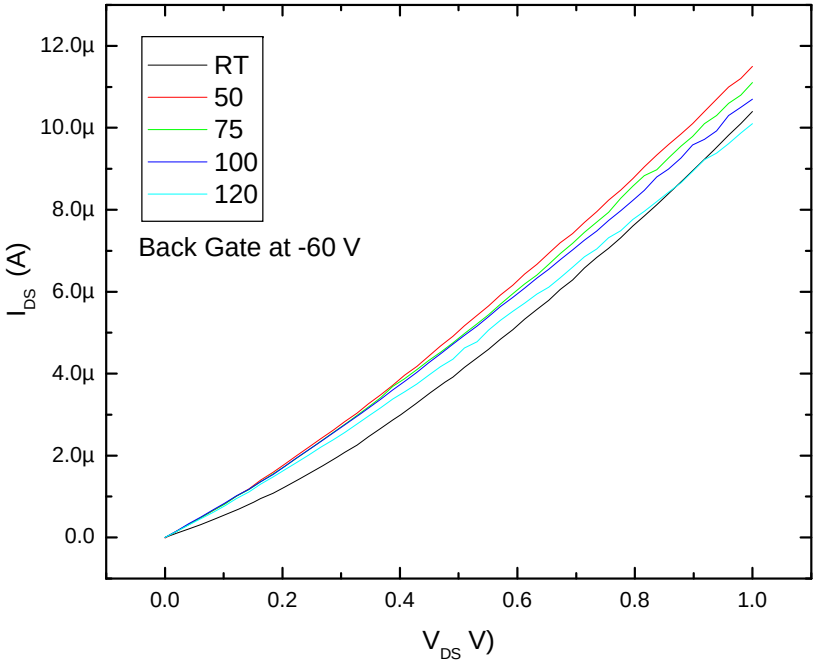
**Schottky Barrier thickness becomes a function of the diode size for small diode ( below 80 nm ) and contribution of tunneling current to the total conductance is greatly enhanced**. [2]


[1] S M Sze. *Physics of Semiconductor Devices*, 2nd ed

[2] Smit G.D.J.et al. *APL* Vol 81,No 20

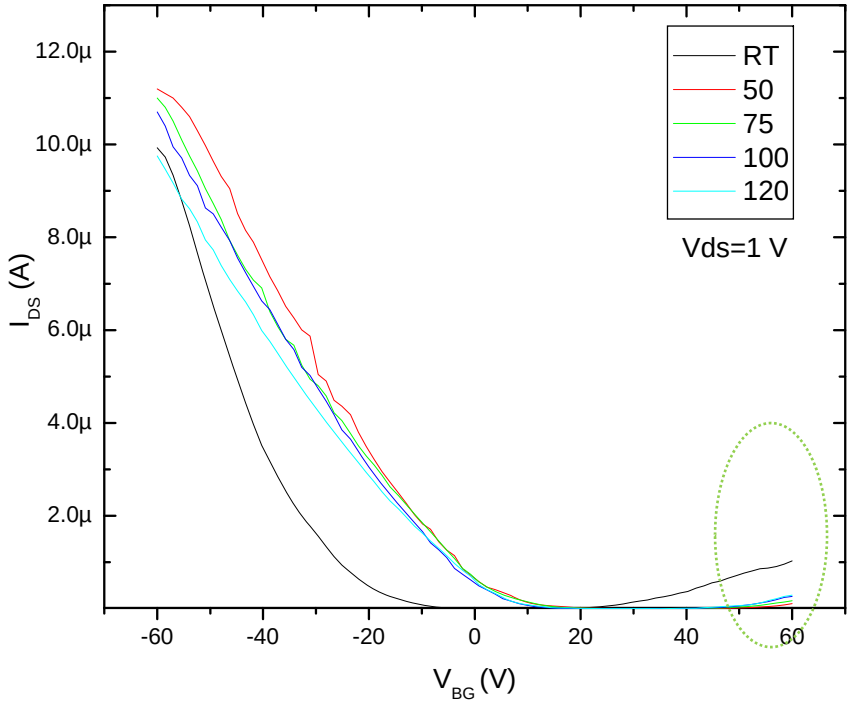
# Temperature Dependant Transport Properties of SiNW at p-type regime

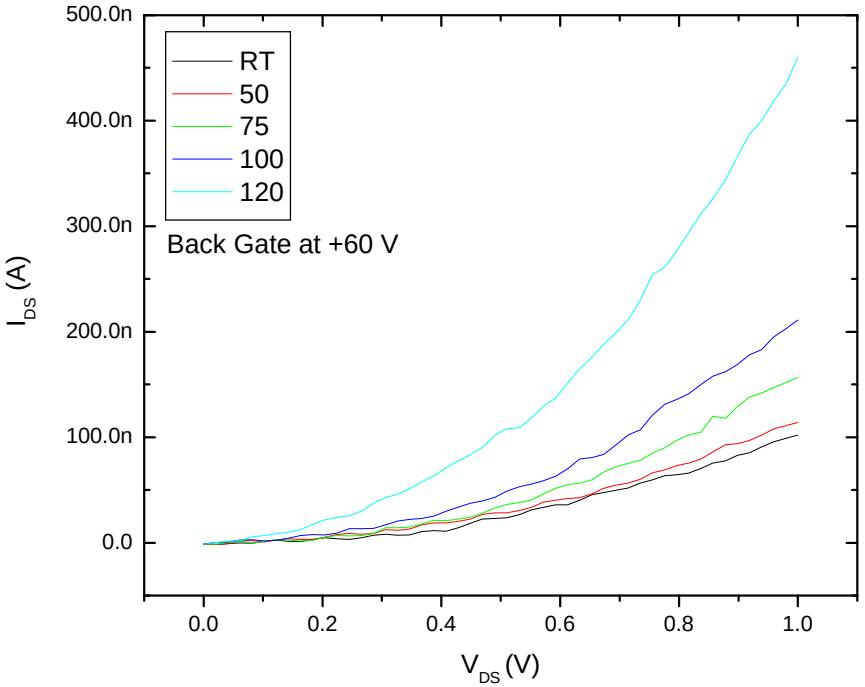



**Current increases from room temperature to 50 C due to increased carrier injection. After that carrier injection is limited by applied voltage but due to phonon scattering  current decreases. For hole transport it is almost ohmic in RT.**

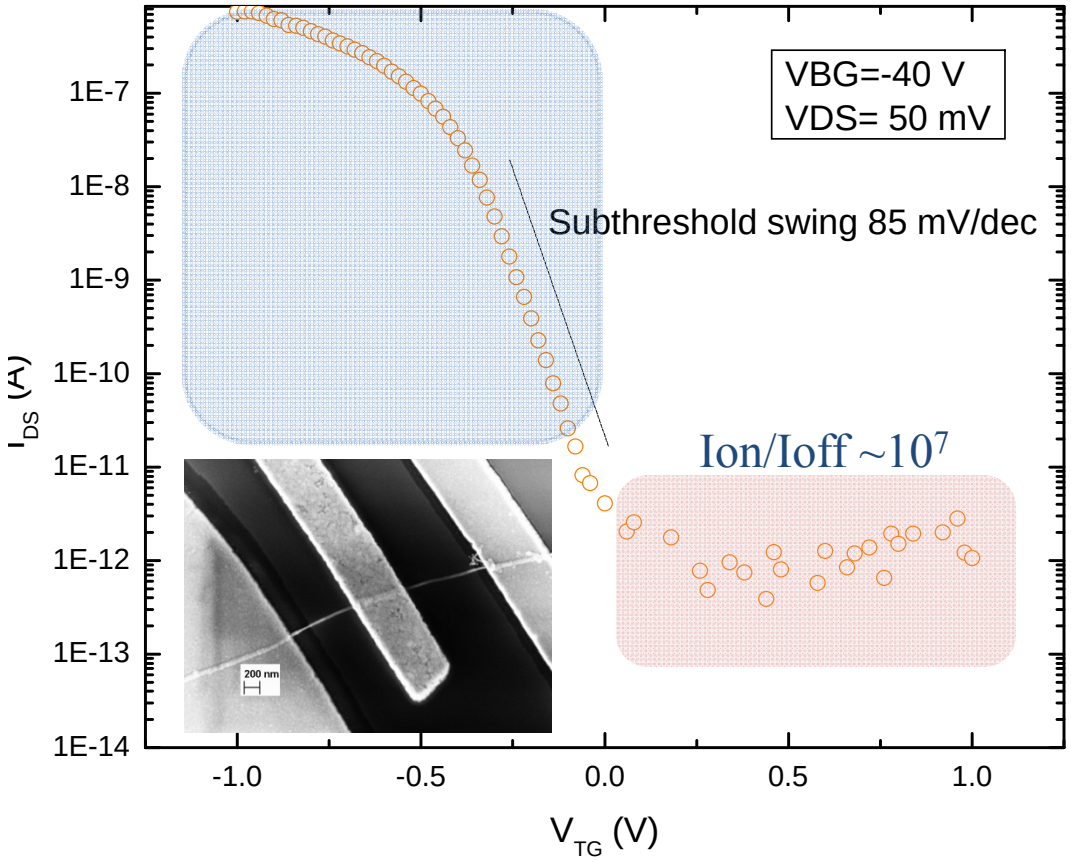
# Temperature Dependant Transport Properties of SiNW at n-type regime



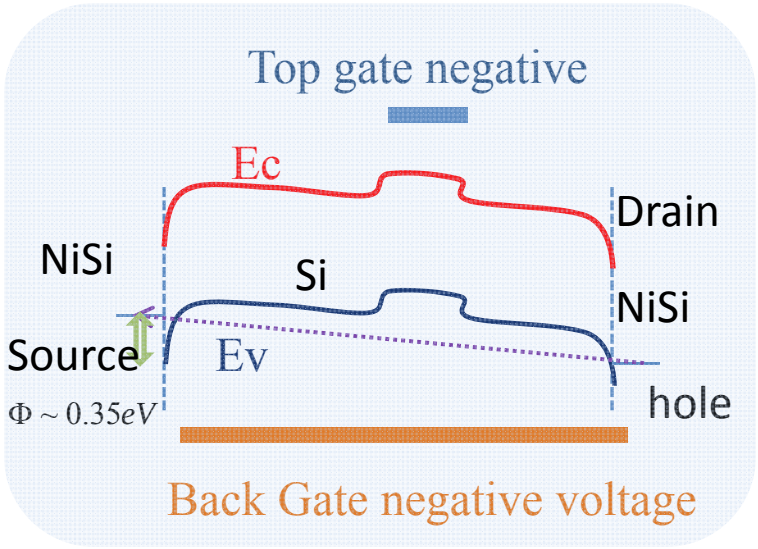



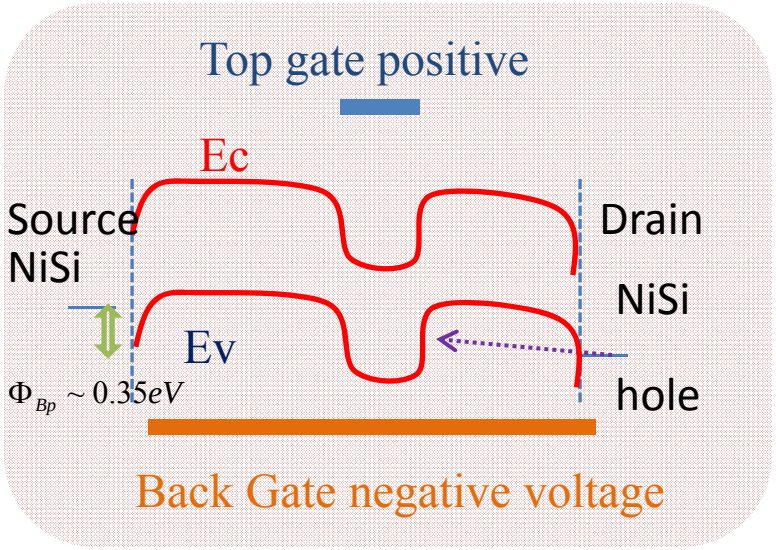

**Current increases from room temperature to 120 C due to increased carrier injection at electron. For electron transport it is always through Schottky Barrier.**

# Top Gated Device Characteristics: p regime

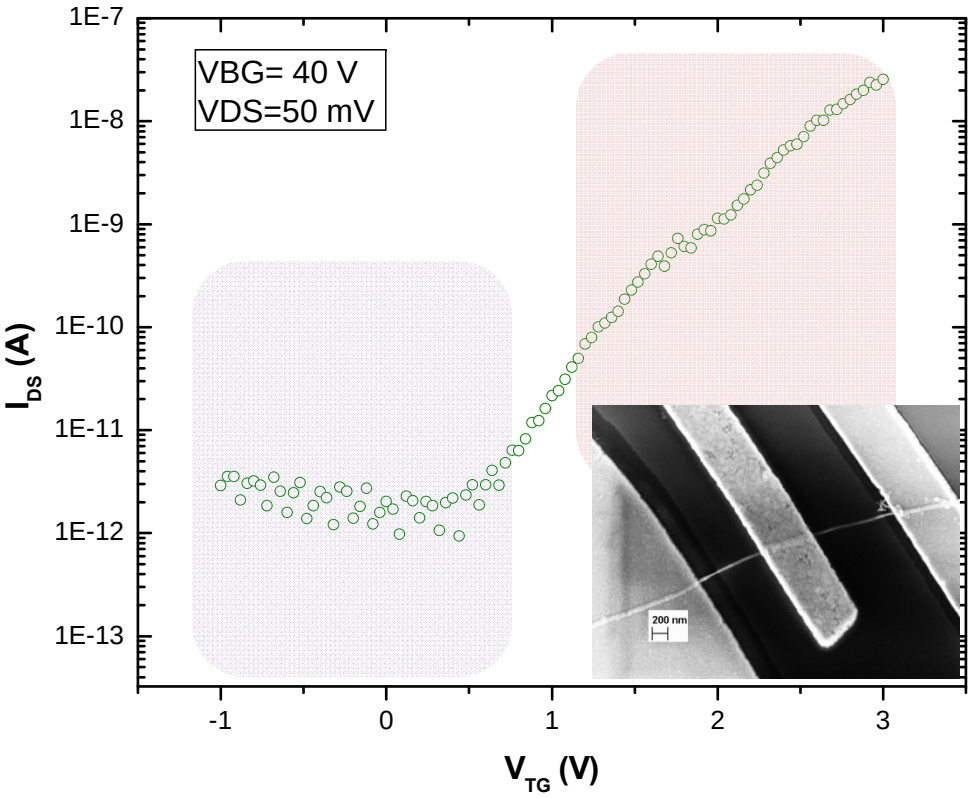



**Drain current vs top gate voltage in p regime .On current is high for hole owing to smaller Schottky barrier height (typically 0.39-0.48 eV). Here also a steep subthreshold swing ( 85 mV/dec) also observed. For 5 nm SiO2 gate which is very good indicating low traps in the interface.**

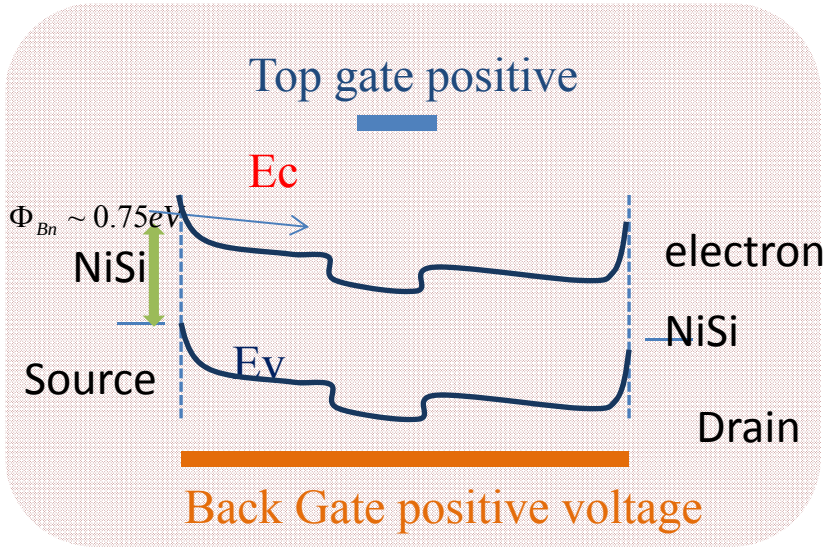


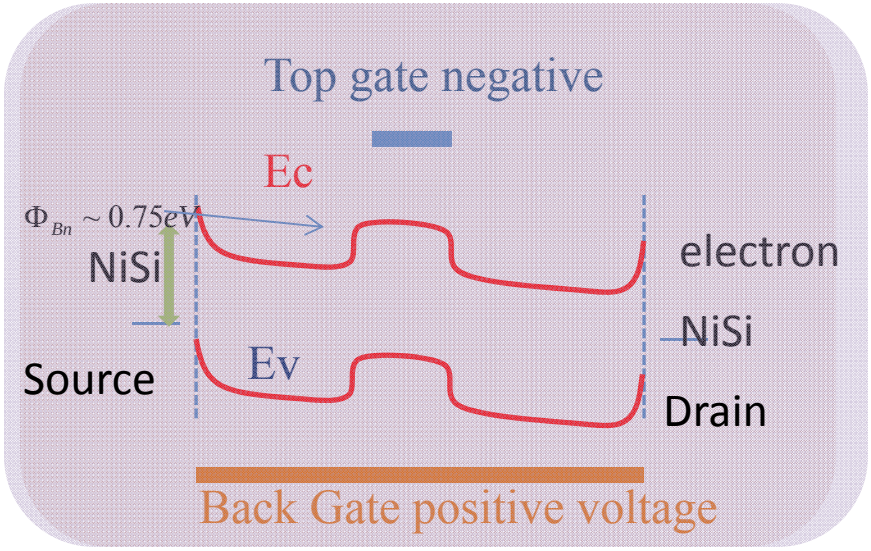



# Top Gated Device Characteristics: n regime




**Drain current vs top gate voltage in n regime. The On current for electron is low due to higher Schottky barrier height (typically 0.66-0.75 eV).The Subthreshold swing is around 480 mV/dec owing to leakage path induced by global back gate.**



# TCAD Simulation of NW

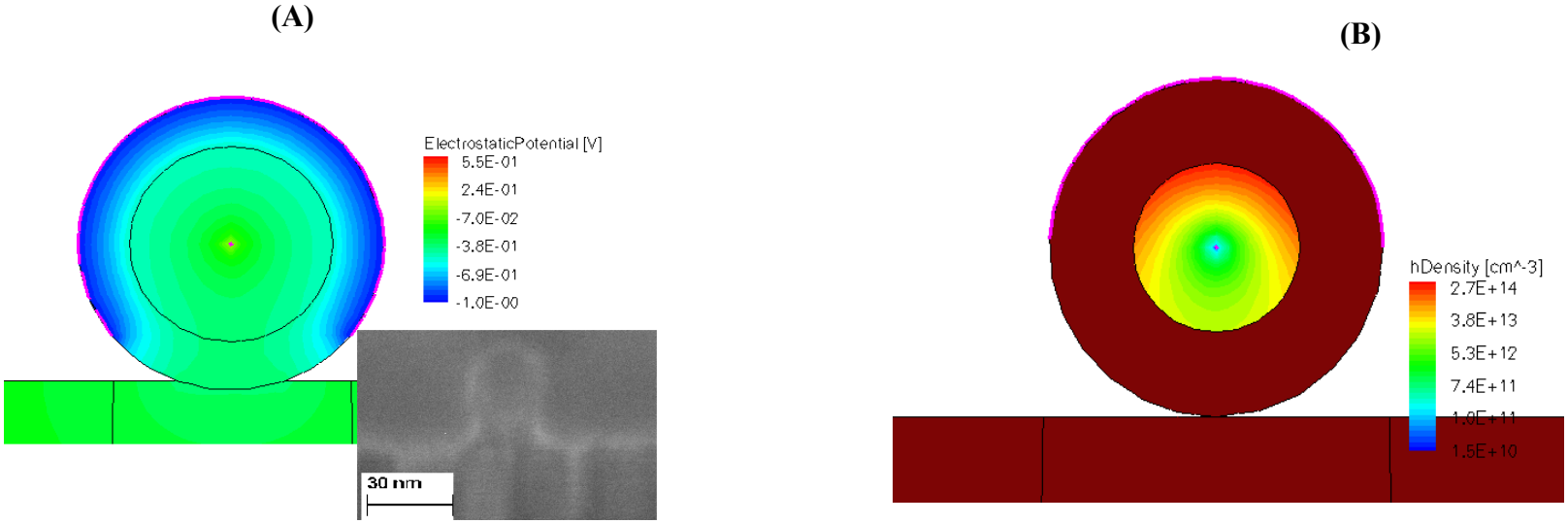
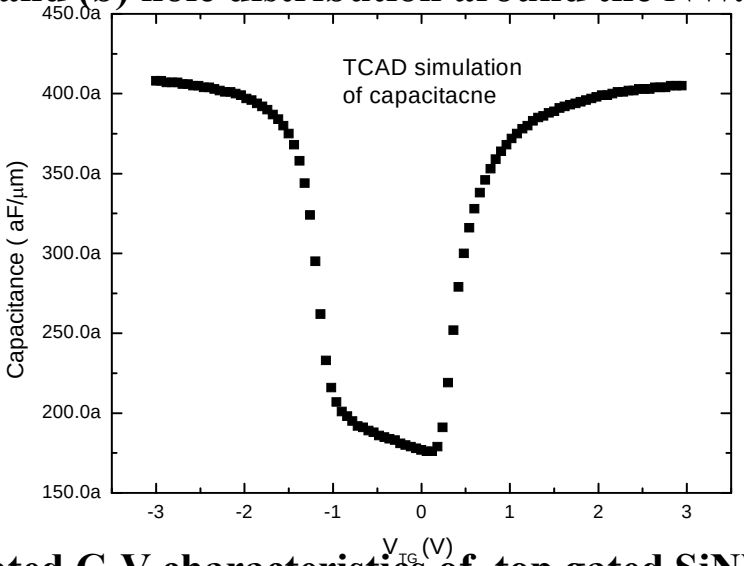
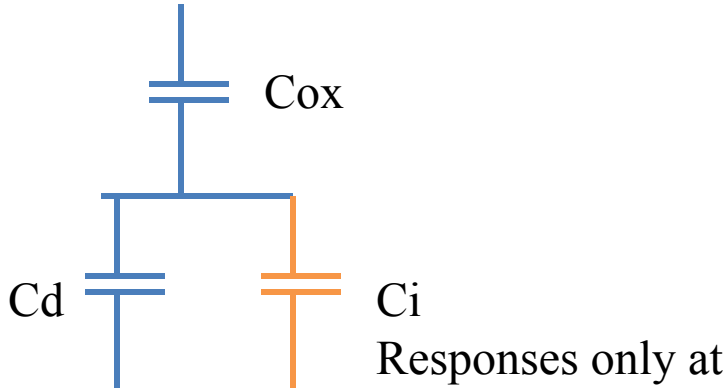


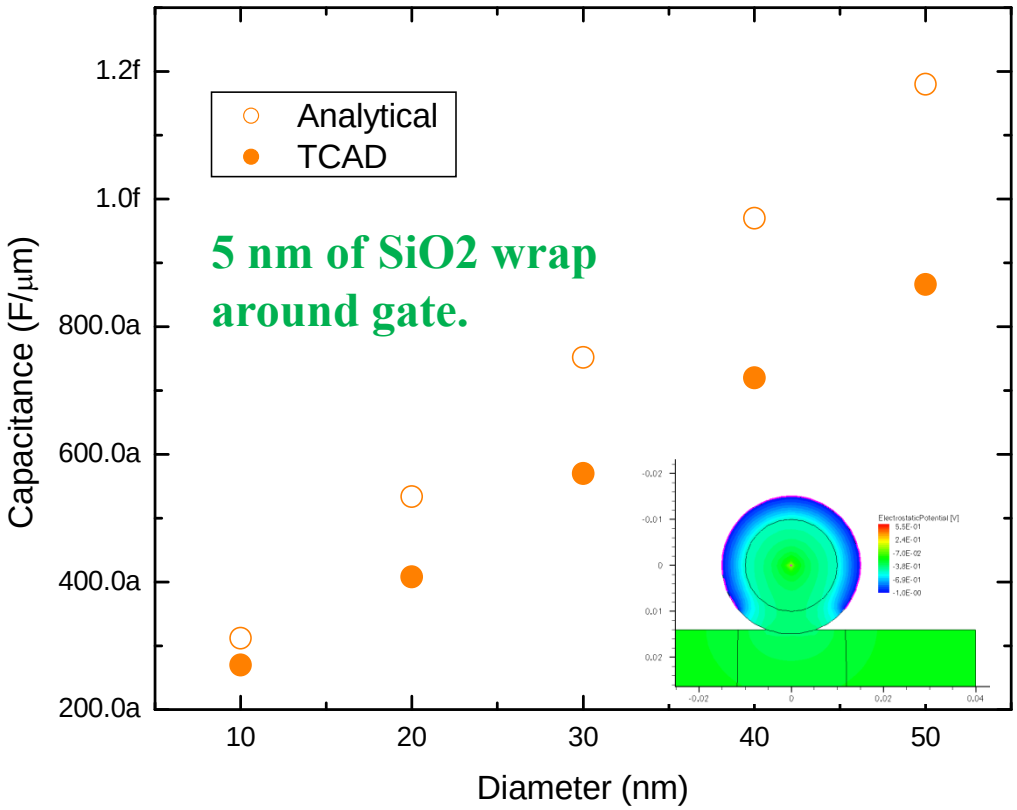

**Figure : TCAD simulation showing (a) electrostatic potential profile, FIB cross section of SiNW and (b) hole distribution around the NW.**




**Simulated C-V characteristics of top gated SiNW.**
**Top gate is varied from -3 to +3 V while back gate is kept at -40 V**

# Capacitance of Silicon Nanowire FET




**Analytical formula for coaxial cylindrical capacitor**

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\left(1+\frac{2t_{ox}}{d_{nw}}\right)}$$

**In TCAD simulation it accounts for gate capacitance as well as semiconductor capacitor and of course the right geometry of the gate can be incorporated. It solves Maxwell EM equation to calculate gate cap and Poisson equation to solve semiconductor cap. Low frequency of 100 Hz signal used at gate.**

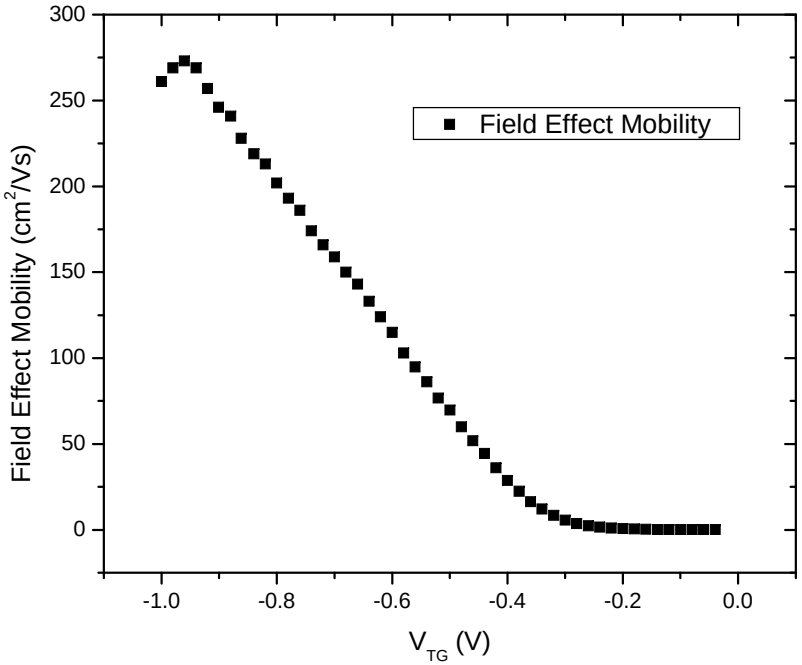
**TCAD modeling gives more accurate estimation of capacitance over any analytical formula.**

# Field Effect Mobility of Silicon Nanowire FET

**For our NW, radius r~10 nm  Lg=700nm**

**Transconductance is defined as** $g_m = \frac{\delta I_{DS}}{\delta V_{GS}}$ **(at Vds=50 mV)**

**Field Effect Mobility,** $\mu = \frac{g_m L^2}{C_{ox} V_{DS}}$ **Which gives peak hole field effect mobility around 265cm²/V.s**




**Mobility**

1. **Hall Mobility**
2. **Field Effect Mobility**
3. **Effective Mobility**

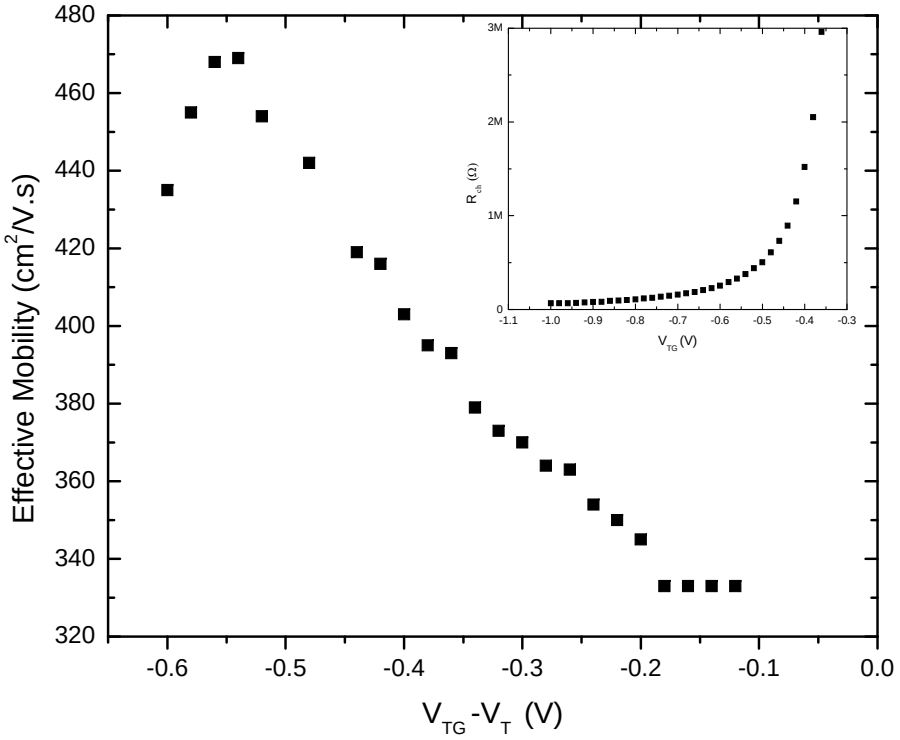
**Mobility calculation restricted to hole only due to ohmic behavior for hole transport**

$\mu_p - V_{GS}$ **Characteristics shows a near identical behavior with mobility increases first before sharply decay due to enhanced surface scattering**

**Figure : Field effect mobility (hole ) as a function of top gate Vgs**

# Effective Mobility of Silicon Nanowire FET

**Effective mobility** $\mu_p = g_D \times \frac{L^2}{C_{ox}} \times \frac{1}{(V_{GS} - V_t)}$ **Where drain conductance** $g_D = \frac{\delta I_{DS}}{\delta V_{DS}}$




The main difference between field effect mobility and effective mobility is the neglect of gate electric field in the field effect mobility expression .

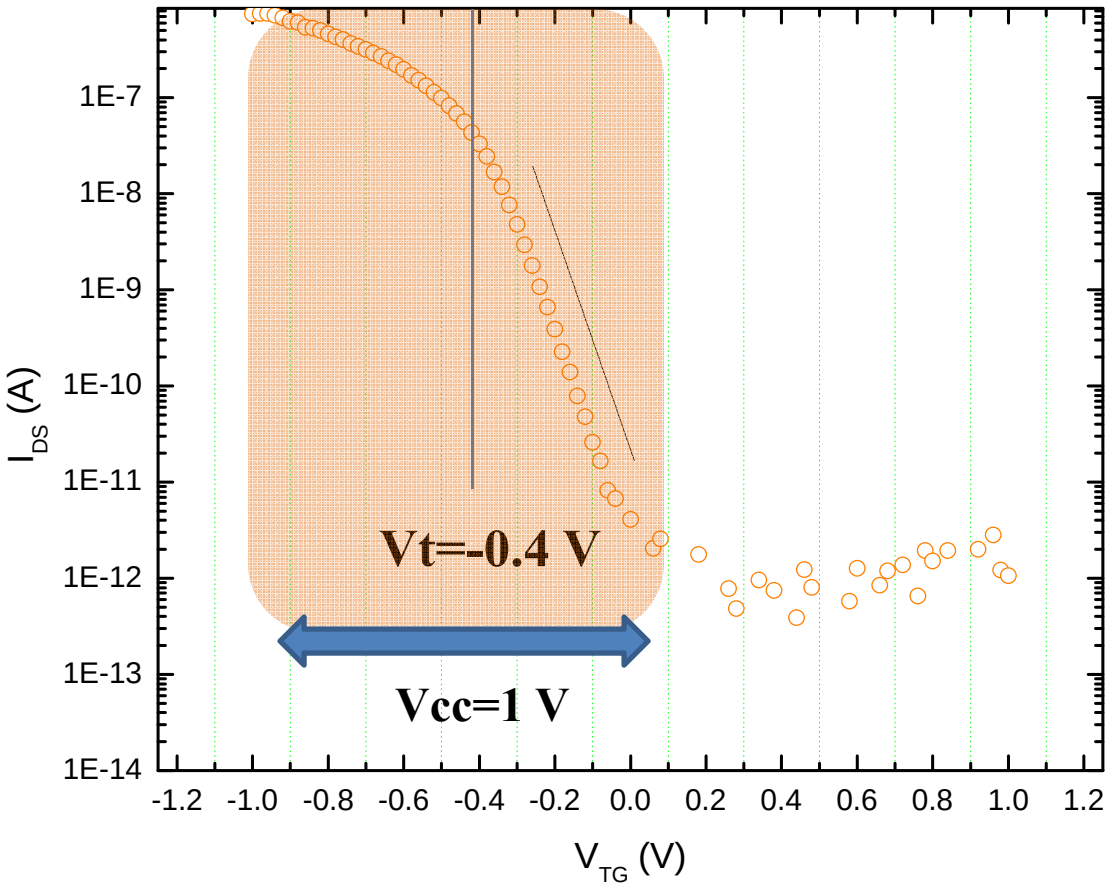
For the device modeling, effective mobility is often used to predict the current and switching speed

**Figure : Effective mobility (hole ) as a function of top gate Vgs. Inset Channel resistance as function of gate voltage**

# Summary of Silicon Nanowire FET Properties

| Length | 700 nm |
|---|---|
| Diameter | 18 nm |
| Threshold Voltage | -400 mV |
| Inverse Substhreshold Swing | 85- 90 mV/dec |
| Ion | 1 uA |
| Ion/Ioff | ~$10^7$ |
| Ron | 66 kΩ |
| Peak Field Effect Mobility (hole) | 265 $cm^2/V.s$ |
| Peak Effective Mobility (hole) | 470 $cm^2/V.s$ |
| Contact | NiSi |
| Contact Behavior | Schottky |

# Benchmarking of Silicon Nanowire FETs




## 4 key metrics

**1.Gate Delay CV/I**
**2.Energy Delay CV/I. $CV^2$ product**

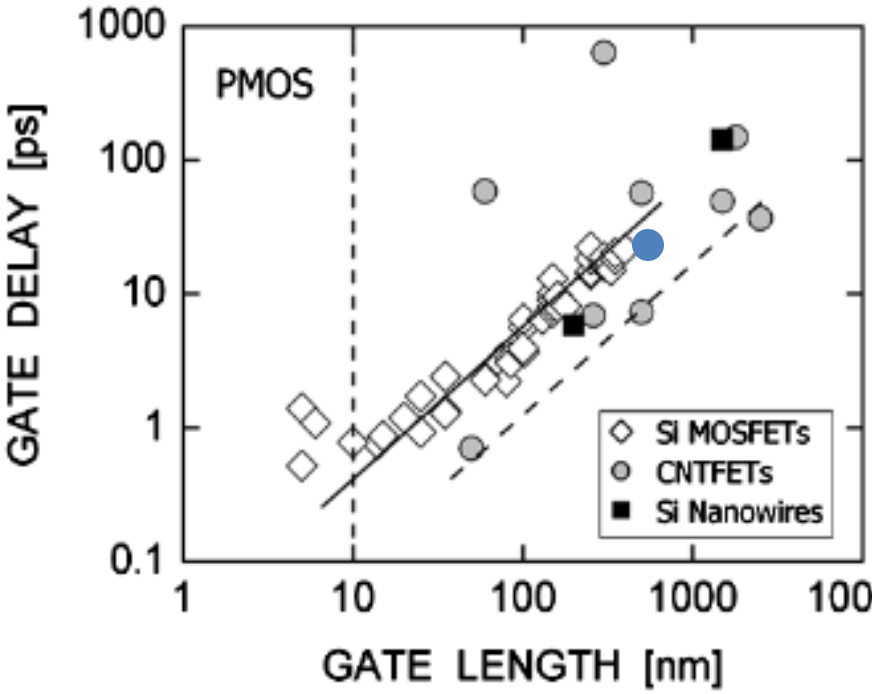
**3.Subthreshold slope**
**4.Ion/Ioff**

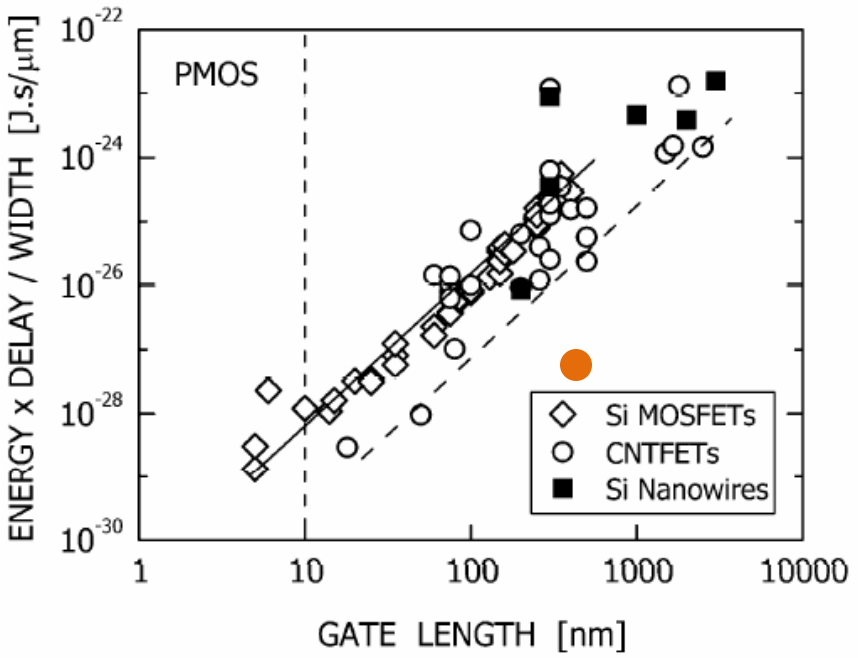
## Benchmarking Method

- **Ion at $V_D$ =Vcc and Vg-Vt=2Vcc/3**
- **Ioff at $V_D$ =Vcc and Vg-Vt=2Vcc/3**
- **Measure or estimate Capacitance**

Ref: Robert Chau et al , IEEE transaction on Nanotechnology, Vol 4 No 3

# Benchmarking of Silicon Nanowire FETs




1. **Gate Delay 19.2 ps**
2. **Energy Delay $2.38 \times 10^{-28}$/um width**
3. **SS slope 85-90 mV/dec**
4. **Ion/Ioff $10^7$**

Ref: Robert Chau et al , IEEE transaction on Nanotechnology, Vol 4 No 3

# Simulation of SiNW

## Poisson's Equation

$$\varepsilon \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) - \rho_S$$

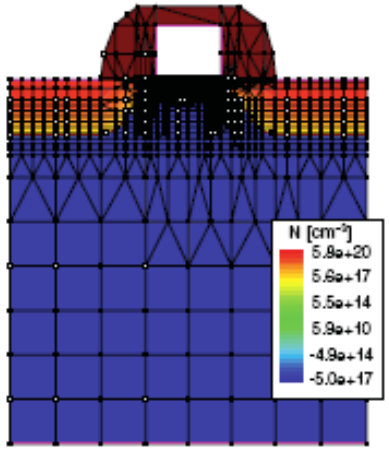
## Boltzman's transport Equation

$$\vec{J}_n = q\mu_n \vec{E}_n n + qD_n \vec{\nabla} n$$

$$\vec{J}_p = q\mu_p \vec{E}_p p - qD_p \vec{\nabla} p$$

$$\vec{E}_n = \vec{E}_p = \vec{E} = -\vec{\nabla} \psi$$

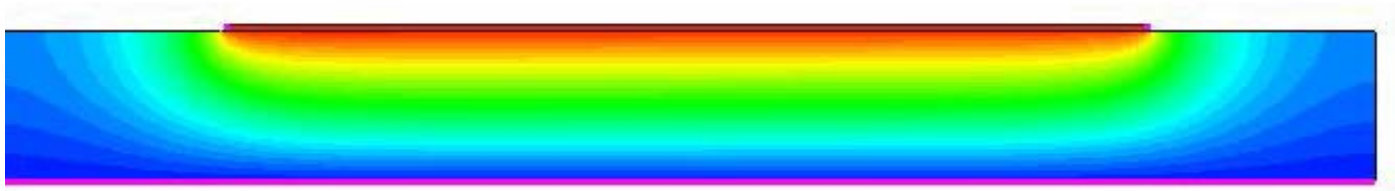
Sentaurus TCAD simulator used that solves Poisson and Boltzman transport equation simultaneously .Many other physical models can be used in addition to this basic model as required.

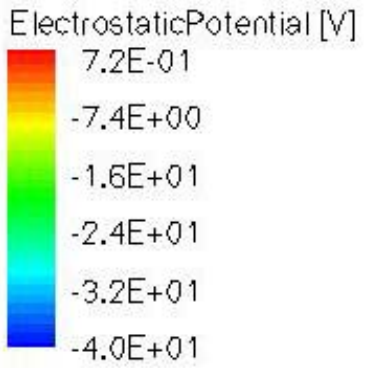


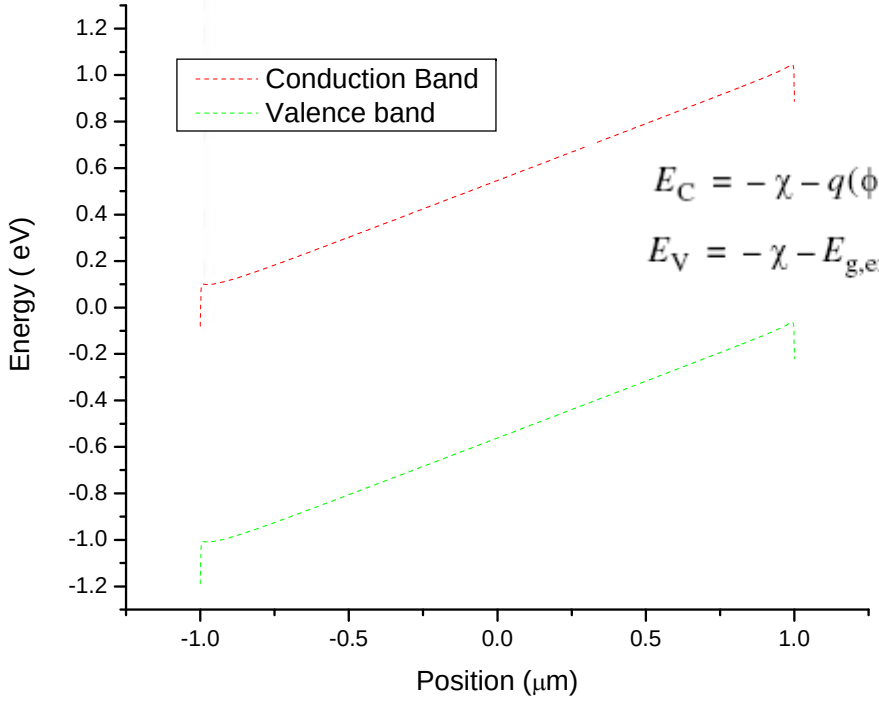

It is a Finite element based modeling software

Ref: www.synopsis.com

# Simulation of SiNW





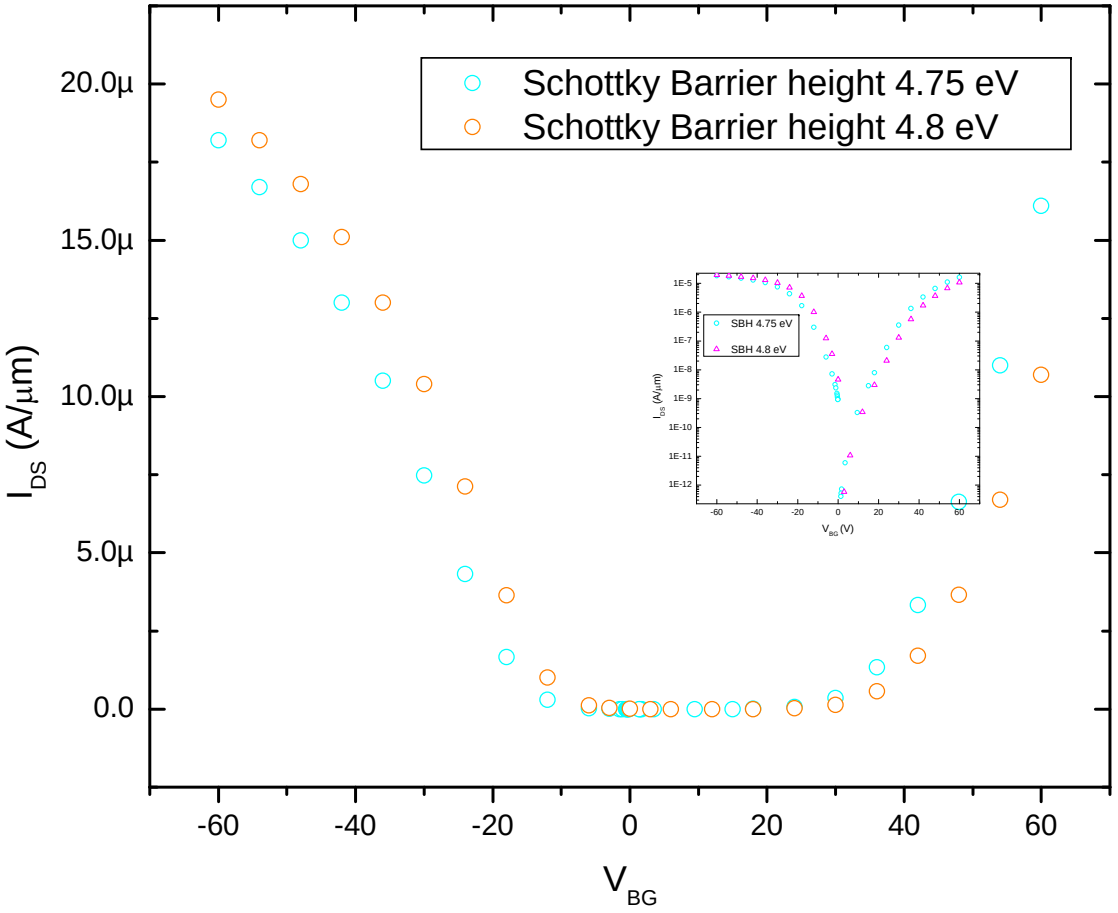



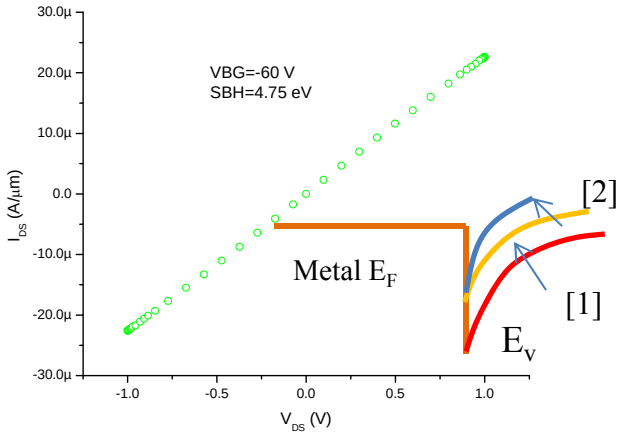

$$E_C = -\chi - q(\phi - \phi_{ref})$$

$$E_V = -\chi - E_{g,eff} - q(\phi - \phi_{ref})$$

Electrostatic profile and energy band profile of a 2 um long and 20 nm diameter SiNW on 300 nm thick SiO2 simulated to get qualitative idea of current transport.

# Simulation of SiNW




Boundary condition for Schottky Barrier

$$\Phi = \Phi_F - \Phi_B + \frac{kT}{q}\ln\left(\frac{N_C}{n_i}\right)$$

Barrier Lowering $\Delta\Phi = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}}$

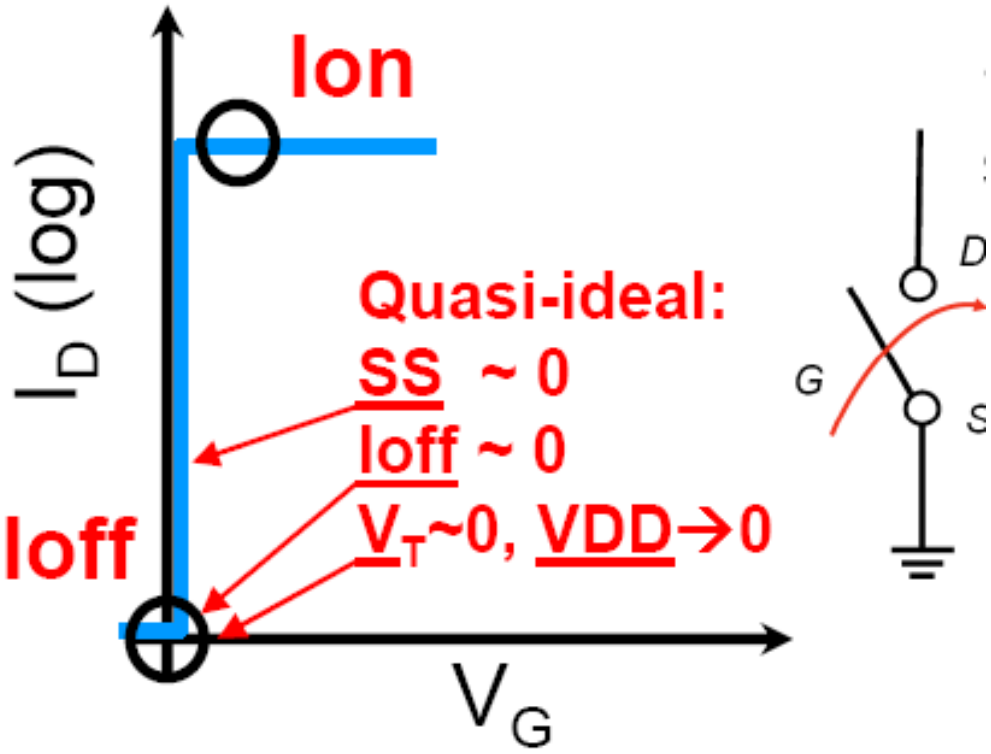
WKB Tunneling Probability

$$\kappa_{c,v}(r,\varepsilon) = \sqrt{2m_c(r)\left|E_{c,v}(r)-\varepsilon\right|}/\hbar$$

Tunneling current $I \sim e^{-2Kd}$

Higher SBH favors hole injection from metal to semiconductor while lower one favors electrons

# Quasi Ideal Switch for Digital Application







Binary Switch

1. Two stable states

2. Ion as high as possible

3.Ioff as low as possible

4.Ion/Ioff >$10^5$

5.Abrupt swing (mV/decade)

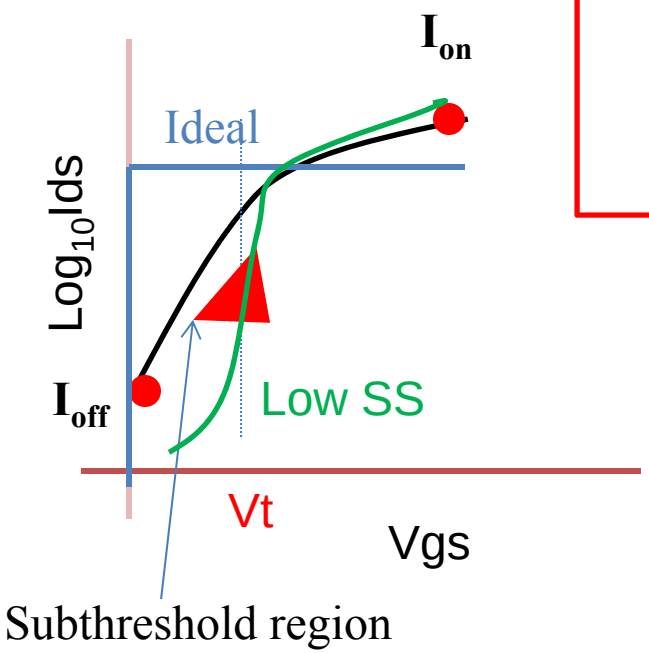
# Tunneling FET

Why 60 mV/Dec limit

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left( \frac{kT}{q} \right)^2 e^{q(V_g - V_t)/mKT} (1 - e^{-qV_{ds}/kT})$$

$$m = 1 + \frac{C_D}{C_{ox}}$$

$$SS = \frac{dV_g}{d(\log_{10} I_d)} = \ln 10 \frac{kT}{q} (1 + \frac{C_{dep}}{C_{ox}} + \frac{C_{ss}}{C_{ox}})$$




$$\ln 10 \frac{kT}{q} = 60 \text{ mV/dec}$$

Carrier injection by lowering the barrier.
Subthreshold current is a diffusion current

Ref: Yuan Taur, Tak Ning. *Fundamental of VLSI Devices*

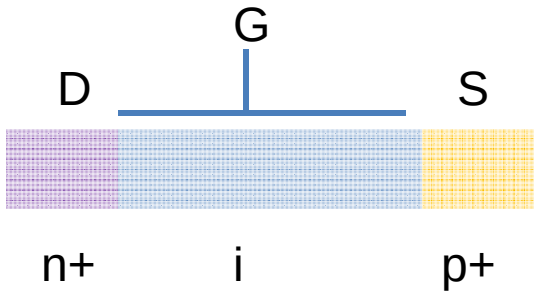
# Tunneling FET: Principle

OFF State

Vd=positive

Vg=0

No Current flows



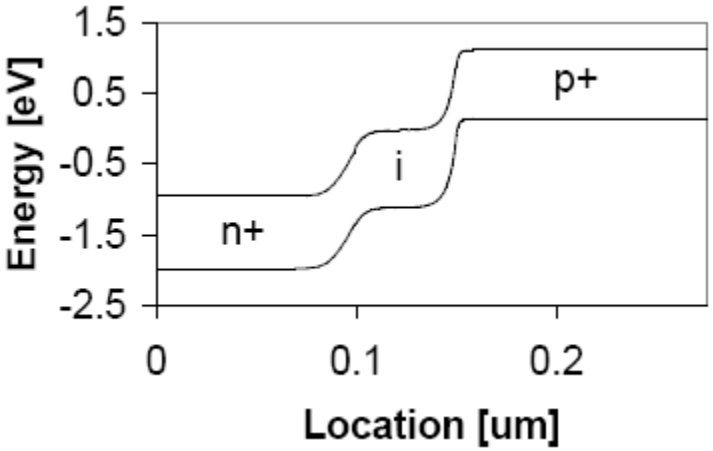

Gated p-i-n junction

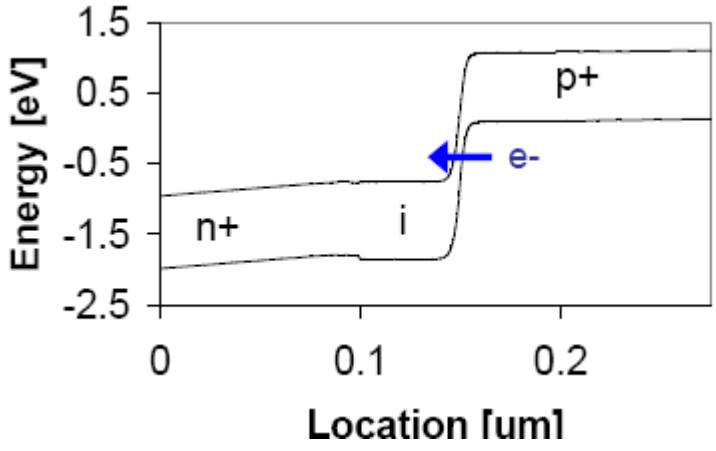
ON State

Vd=positive

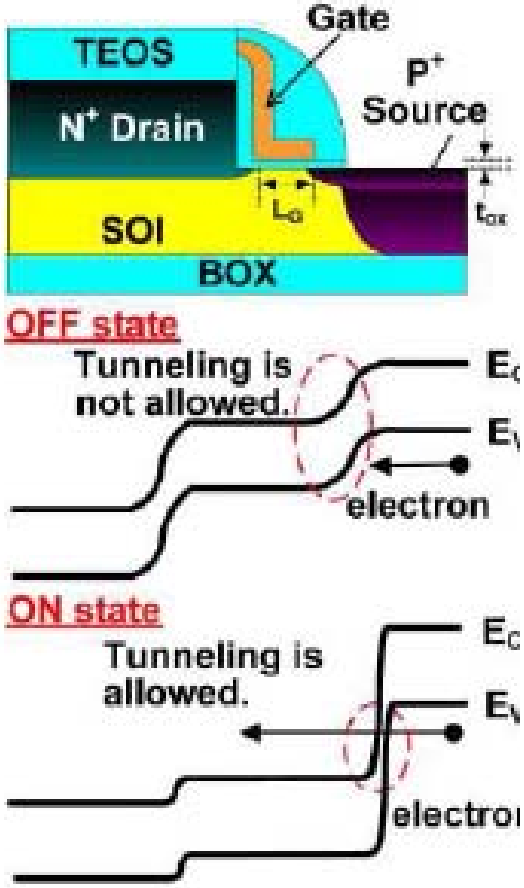
Vg=positive

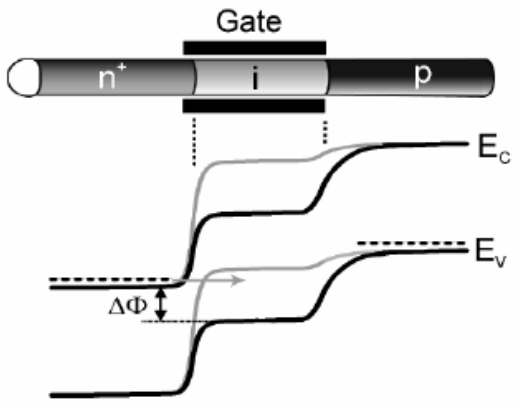
Barrier thins current flows

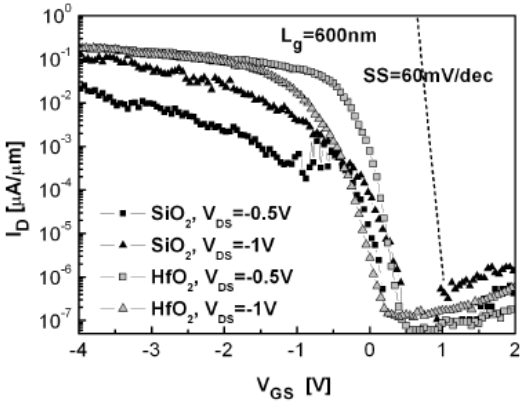


# Tunneling FET



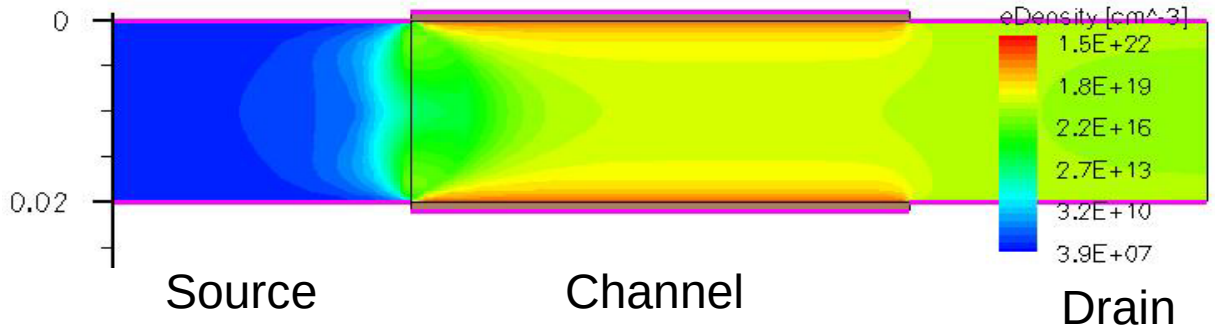

$I_{on}$=0.3 uA/um
$I_{on}/I_{off}$=$10^5$

Design is complex: Require High and abrupt doping in source and drain region And sometime non standard CMOS process flow

$I_{on}$=12uA/um
$I_{off}$=5.4 nA/um

*Ref: K Moselund at al ESSDERC 2009*

# Tunneling FET Simulation




## Design of TFET

1.Intrinsic Silicon body of 1 um length and 20 nm diameter

2. Schottky contact of NiSi of SBH 4.75 eV

3.High K dielectric $HfO_2$ 1 nm

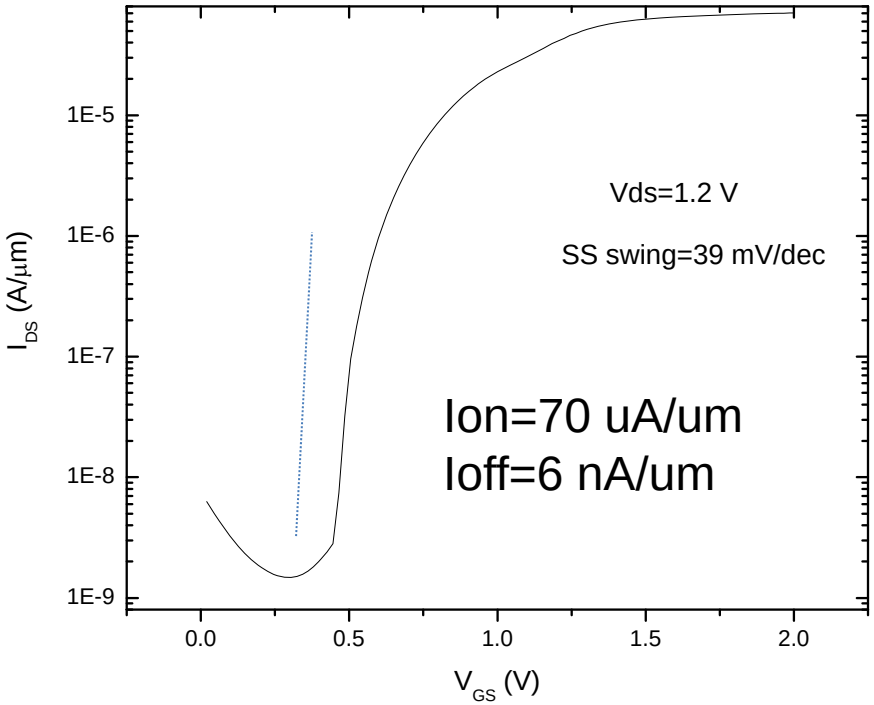
## Simulation Consideration

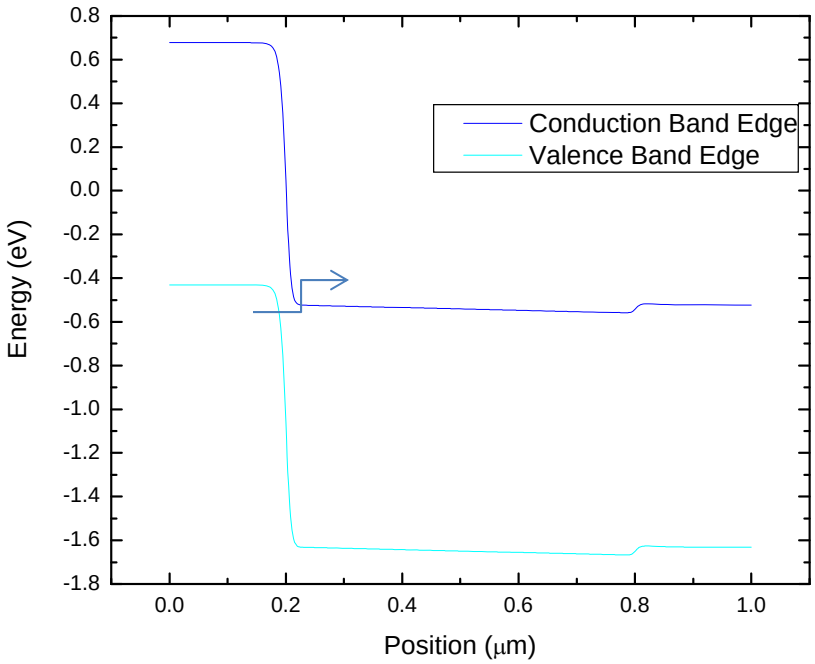
$$\kappa_{c,v}(r,\varepsilon) = \sqrt{2m_c(r)\left|E_{c,v}(r) - \varepsilon\right|}/\hbar$$

WKB Tunneling Probability $T=e^{-2kL}$

Tunneling mass for electron $0.19m_o$ and $0.16m_o$ for hole

# Tunneling FET Simulation




With this simple design where no doping is necessary we achieved very good SS swing of 39 mV/dec

# Summary of Accomplishments

1. **I have successfully fabricated Silicon Nanowire based FET devices to study their transport behavior.**
2. **I have implemented more rigorous approach such as taking care of silicidation effect in NW channel and capacitance extraction by TCAD simulation for data extraction such as mobility, subthreshold swing.**
3. **I have studied temperature dependant carrier transport in SiNW.**
4. **I have demonstrated superior SiNW devices in terms of High on current , High On/Off ratio and steep subthreshold swing and low on resistance.**

*…Continued*

# Summary of Accomplishments

6. **I demonstrated that TCAD simulation instead of any analytical formula gives accurate estimation of gate capacitance in a top gate form.**
7. **I demonstrated very high mobility owing to better oxide interface quality.**
8. **Simulation is carried out to shed light on carrier transport in NW.**
9. **A new and simple design for tunneling FET is proposed with intrinsic SiNW which demonstrates better swing in subthreshold regime.**

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- Dr Kiki Minoglou, Mentor (IMEC, Belgium)
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